AN13106
Migration guide from i.MX RT1060 to i.MX RT1170

Rev. 1 — February 18, 2021

by: NXP Semiconductors

1   Introduction

This document describes key differences and new features on i.MX RT1170, compared with i.MX RT1060. This document can be used as the migration reference. It is intended for audience:

- who have developed some projects based i.MX RT1060 and decided to migrate the project into i.MX RT1170.

- who is familiar with i.MX RT1060 and want to start the new project based on previous knowledge on i.MX RT1060.

Contents

2 SOC comparison

Table 1 lists the SOC comparisons. Text in red is new features on i.MX RT1170.

Table 1. SOC comparison

Items for comparison	i.MX RT1060	i.MX RT1170
Core and on-chip RAM		
Core 0	CM7 @ Up to 600 MHz 32 KB I-Cache 32 KB D-Cache	CM7 @ Up to 1 GHz 32 KB I-Cache 32 KB D-Cache
Core 1	—	CM4 @ Up to 400 MHz 16 KB I-Cache 16 KB D-Cache
FLEX RAM	512 KB	512 KB
OCRAM	512 KB	512 KB + 128 KB OCRAM1 512 KB + 128 KB OCRAM2 256 KB (Shared with CM4 TCM)
External memory interface		
SEMC - SDRAM	8/16-bit SDRAM up to 166 MHz	8/16/32-bit SDRAM Up to 200 MHz
SEMC - NAND	8/16-bit SLC NAND FLASH	8/16-bit SLC NAND FLASH
SEMC - Parallel NOR FLASH/SRAM	Up to 16 bit	Up to 16 bit
uSDHC - SD/eMMC	eMMC 4.5/SD 3.0	eMMC 5.0/SD 3.0
Flex SPI	2	2
Flex SPI - Width	Up to 8 bit	Up to 16 bit
Flex SPI - Single/Dual/Quad SPI interface	√	√
Flex SPI - Hyper	√	√
Flex SPI - PSRAM	—	√
Flex SPI - OCT interface with XIP support	√	√
Graphic, Display & Camera		
LCDIF	√	√
LCDIFv2	—	√

Table continues on the next page...

Table 1. SOC comparison (continued)

Items for comparison	i.MX RT1060	i.MX RT1170
PXP	√	√
GPU	—	√
Parallel CSI	√	√
Parallel DSI	√	√
MIPI CSI	—	√
MIPI DSI	—	√
Connectivity		
USB	2	2
10/100M ENET with IEEE1588	2	1
1G ENET with AVB	—	1
1G ENET with TSN	—	1
UART	8	12
LPSPI	4	6
I2C	4	6
FlexCAN	3	3
FlexIO	3	2
EVMSIM	—	2
GPIO	149	174
Audio		
SAI	3	4
SPDIF	1	1
ASRC	—	1
PDM MIC	—	1
MQS	1	1
Timer		
WDOG	4	5

Table continues on the next page...

Table 1. SOC comparison (continued)

Items for comparison	i.MX RT1060	i.MX RT1170
GPT	6	6
QDC	4	4
QTimer	4	4
FlexPWM	4	4
PIT	1	2
Analog		
ACMP	4	4
ADC	2	0
LPADC	0	2
ADC ETC	1	1
DAC	0	1
TSC	1	0
Others		
eDMA	1	2
8 × 8 Keypad	√	√
Security	√	√

3 Package

As shown in Table 2, i.MX RT1170 is a 289-pin MAPBGA while i.MX RT1060 is a 196-pin MAPBGA. i.MX RT1170 has a larger package in order to accommodate additional functionality and change to the power architecture.

Table 2. Package comparison

	RT1060	RT1170
Package	196-pin MAPBGA	289-pin MAPBGA

4 Pin mux

For the new pin mux on i.MX RT1170, user can refer to Table 3.

Table 3. Pin mux information/tools

Pin mux information/tools	Comments
Muxing Options table in RM	Give pin list information for a peripheral.
Pin Assignments in RM	Give pin mux list information on a pin and also show pad setting.
Pin Assignments in excel format	This table is in the attachment of this document as an option for pin assignment.
Pin config tool in MCUXpresso or standalone tools	A powerful graphic tool help customer to assign pin for application.

5 Power supply change

The following describes key differences between i.MX RT1170 and RT1060. For details, see *Hardware Development Guide for the MIMXRT1170 Processor* (document MIMXRT1170HDUG) and *MIMXRT1170 EVK Board Hardware User's Guide* (document MIMXRT1170EVKHUG).

- i.MX RT1170 has more power domains than RT1060, especially introduces `NVCC_LPSR` domain. You will see during power up sequence only if `VDD_LPSR_DIG` is stable, `VDD_SOC_IN` can be applied after 1 ms delay.
- i.MX RT1170 uses POR pin reset in `VDD_SNVS_DIG` (1.8 V) domain, which means to add external pull up or to use external POR logic, guarantee the voltage level first.
- i.MX RT1170 internal DCDC has two outputs, `VDD_DIG` for core platform and 1.8 V for chip supply. i.MX RT1060 has only one output.
- i.MX RT1170 is an automotive grade product and the internal DCDC load capacity is limited, so external PMIC is required to power the core platform. For RT1060, internal DCDC is suggested for different standard products.

6 Clock

6.1 Overview

i.MX RT1170 clock architecture is new. It consists of three parts:

- Crystal/OSC/PLL/PLL_PFD as clock source
- Available clock source for each clock root and divider setting
- Clock gate

For more important information related to the below, see *i.MX RT1170 Processor Reference Manual* (document IMXRT1170RM).

- **System Clocks Table**: Gives the IP clock mapping to system clock source.
- **Clock Tree**: Gives the clock path from clock source to each root clock.
- **Clock Sources Table**: Lists all possible clock sources.
- **Clock Root Table**: Give the available clock source for each root clock.
- **Clock Gate Table**: Lists all the gate control.
- **Clock Group**: Lists all the clock groups (Synchronized clock).

6.2 Oscillator & PLL

Table 4. Oscillator & PLL comparison

Oscillator & PLL	RT1060	RT1170
Crystal Oscillator 24 MHz	√	√
Crystal Oscillator 32 KHz	√	√
RC Oscillator 32 KHz	√	√
RC Oscillator 16 MHz	—	√
RC Oscillator 24 MHz	√	—
RC Oscillator 48 MHz	—	√
RC Oscillator 400 MHz	—	√
PLL1	ARM PLL (Up to 600 MHz core)	ARM PLL (Up to 1 GHz core)
PLL2	SYS PLL (Dedicated 528 MHz)	SYS PLL1 Dedicated 1 GHz)
PLL3	USB1 PLL (Dedicated 480 MHz)	SYS PLL2 (Dedicated 528 MHz)
PLL4	AUDIO PLL (650-1300 MHz)	SYS PLL3 (Dedicated 480 MHz)
PLL5	VIDEO PLL (650-1300 MHz)	AUDIO PLL (650-1300 MHz)
PLL6	ENET PLL (Dedicated 500 MHz)	VIDEO PLL (650-1300 MHz)
PLL7	USB2 PLL (Dedicated 480 MHz)	—

7 Power mode/management

Compared with i.MX RT1060, i.MX RT1170 is based on brand new power architecture. For more details, see *i.MX RT1170 Processor Reference Manual* (document IMXRT1170RM) and *Debug and Application for RT1170 Clock and Low Power Feature* (document AN13104).

8 DMA

Table 5. DMA for i.MX RT1060 and i.MX RT1170

Items for comparison	i.MX RT1060	i.MX RT1170
eDMA (32 channel)	√	√
eDMA_LPSR (32 channel)	—	√

9 Memory map

Table 6 lists some key memory maps for comparison. For more detailed information, see *i.MX RT1170 Processor Reference Manual* (document IMXRT1170RM).

Table 6. Memory map for on chip/external memory

Items for comparison	i.MX RT1060	i.MX RT1170
CM7 FLEX RAM ITCM	`0x0000_0000` - `0x0001_FFFF` (Default 128 KB)	`0x0000_0000` - `0x0003_FFFF` (Default 256 KB)
CM7 FLEX RAM DTCM	`0x2000_0000` - `0x2001_FFFF` (Default 128 KB)	`0x2000_0000` - `0x2003_FFFF` (Default 256 KB)
CM7 OCRAM (mapping from CM4 TCM)	—	`0x2020_0000` - `0x2023_FFFF` (256 KB)
CM7 OCRAM1	`0x2020_0000` - `0x2027_FFFF` (512 KB)	`0x2024_0000` - `0x202B_FFFF` (512 KB)
CM7 OCRAM2	—	`0x202C_0000` - `0x2033_FFFF` (512 KB)
CM7 OCRAM1 ECC	—	`0x2034_0000` - `0x2034_FFFF` (64 KB)
CM7 OCRAM2 ECC	—	`0x2035_0000` - `0x2035_FFFF` (64 KB)
CM7 OCRAM(FLEX RAM ECC)	—	`0x2036_0000` - `0x2037_FFFF` (128 KB)
CM7 FLEX RAM OCRAM	`0x2028_0000` - `0x2028_FFFF` (Default 256 KB)	`0x2038_0000` - `0x2038_0000` (Default 0 KB, maximum 512 KB)
CM4 ITCM	—	`0x1FFE_0000` - `0x1FFF_FFFF` (128 KB)
CM4 DTCM	—	`0x2000_0000` - `0x2001_FFFF` (128 KB)
CM4 OCRAM (From CM4 TCM)	—	`0x2020_0000` - `0x2023_FFFF` (256 KB)
CM4 OCRAM1	—	`0x2024_0000` - `0x202B_FFFF` (512 KB)
CM4 OCRAM2	—	`0x202C_0000` - `0x2033_FFFF` (512 KB)
CM4 OCRAM1 ECC	—	`0x2034_0000` - `0x2034_FFFF` (64 KB)
CM4 OCRAM2 ECC	—	`0x2035_0000` - `0x2035_FFFF` (64 KB)
CM4 OCRAM(From FLEX RAM ECC)	—	`0x2036_0000` - `0x2037_FFFF` (128 KB)
CM4 OCRAM (From CM7 FLEX RAM)	—	`0x2038_0000` - `0x2038_0000` (Default 0 KB, maximum 512 KB)
SEMC	`0x8000_0000` - `0xDFFF_FFFF` (1.5 GB)	`0x8000_0000` - `0xDFFF_FFFF` (1.5 GB)
FlexSPI1	`0x6000_0000` - `0x6FFF_FFFF` (256 MB)	`0x3000_0000` - `0x3FFF_FFFF` (256 MB)
FlexSPI2	`0x7000_0000` - `0x7EFF_FFFF` (240 MB)	`0x6000_0000` - `0x6FFF_FFFF` (256 MB)

10 ECC

Table 7 lists ECC feature comparison.

Table 7. ECC comparison

Items for comparison	i.MX RT1060	i.MX RT1170
FLEX RAM ECC	—	√
OCRAM MECC64	—	√
External XECC	—	√

11 Graphic and display

11.1 Graphics Processing Unit (GPU2D)

Graphics Processing Unit (GPU) provides high performance, low-power consumption, and high-quality graphics. It supports raster, vector graphics encompassing most of the embedded graphics use-case scenarios. The following hardware platform and operating system independent APIs are provided. These APIs provide user controls for optimizing the acceleration capabilities available with GPU.

- OpenVG 1.1 API Standard for Vector Graphics Acceleration
- VGLite Graphics API

11.1.1 OpenVG 1.1 API standard for vector graphics acceleration

OpenVG is a royalty-free, cross-platform API managed by Khronos Group. It provides a low-level hardware acceleration interface for vector graphics libraries such as Flash and SVG. OpenVG is used for acceleration of high-quality vector graphics for user interfaces and text on small screen devices.

11.1.2 VGLite graphic API

The GPU can also be used with the VGLite Graphics API. It is designed to support menu-driven user interfaces optimized for a system's overall resource requirements. The goal is to provide maximum performance and keep the memory footprint to a minimum. It has a feature set smaller than required to pass Khronos OpenVG CTS. Supported features include: Porter-Duff Blending, Gradient Controls, Fast Clear, Arbitrary Rotations, Path Filling rules, Path painting, and Pattern Path Filling.

The VGLite API is partitioned to provide controls for following functionalities:

- **Initialization**: For Hardware and Software initialization
- **Pixel Buffers Management**: For GPU surface buffer allocate/free
- **Matrix control**: For transformation including rotation, scale, and translate
- **Blit**: For Raster rendering with compositing, blending, CSC, etc.
- **Vector Path Control**: For 2D path data setup
- **Draw**: For Draw operations

The VGLite Graphics API document is available as a part of the Software Development Kit (SDK).

11.2 LCDIFv2

LCDIFv2 is a new graphic IP on i.MX RT1170 with the following features:

- Display layers can support up to maximum eight layers of alpha blending.
  - One Background (BG) layer for static background image
  - One Foreground (FG) layer for video

— Six User Interface (UI) layers for the icons, test, moving pointers etc.

— The UI layers are for small objects which can be stored in OCRAM.

— The index color (1/2/4/8 bpp) support for each layer and lookup with separate. Color Look-Up Table (CLUT) memory to 32 bits ARGB pixel.

- Each layer supports:

    — Programmable plane size, Width/Height/Pitch, and X/Y offset on the panel.

    — Background color for plane graphics

    — Embedded alpha and global alpha

    — Index color, 1/2/4/8 bpp

    — Other layer encoding formats:

        ◦ RGB565/ARGB1555/ARGB4444

        ◦ YCbCr422, supporting up to two YCbCr layers in blending operation

        ◦ RGB888/ARGB8888/ABGR8888

- Support one parallel camera interface input and the following data formats of CSI-2:

    — YUV422/RGB888/RGB666/RGB565/RGB555/RGB444

12 Audio

12.1 ASRC

The Asynchronous Sample Rate Converter (ASRC) is a new IP on i.MX RT1170 which converts the sampling rate of a signal associated with an input clock into a signal associated with a different output clock.

The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120 dB THD+N and supports up to three sampling rate pairs.

The incoming audio data to this chip may be received from various sources at different sampling rates. The outgoing audio data of this chip may have different sampling rates and it can be associated with output clocks that are asynchronous to the input clocks.

12.2 PDM MIC interface

i.MX RT1170 has a new feature which supports four lanes up to eight channel of PDM D-MIC audio input.

Features:

- Decimation filters

    — Fixed filtering characteristics for audio application

    — 24-bit signed filter output

    — Dynamic range: <140dB at 1KHz tone (0dBFS); per AES17

    — Internal clock divider for a programmable PDM clock generation

    — Full or partial set of channels operation with individual enable control

    — Programmable decimation rate

    — Programmable DC remover

    — Range adjustment capability

    — FIFOs with interrupt and DMA capability

        ◦ Each FIFO with 8 entries length

- Hardware Voice Activity Detector (HWVAD)

  — Interrupt capability

  — Zero-Crossing Detection (ZCD) option

13 Low speed peripherals

13.1 FlexIO

Table 8. FlexIO

Items for comparison	i.MX RT1060	i.MX RT1170
Instance count	3	2
Port size	Up to 32 bit	Up to 32 bit
Shifter count	4	8
Timer count	4	8

14 EMVSIM

Relative to i.MX RT1060, the EMVSIM module is a new IP on i.MX RT1170 which supports the following features:

- Independent clock for SIM logic (transmitter + receiver) and independent clock for register read-write interface
- 16 byte deep FIFO for transmitter and receiver
- Automatic NACK generation on parity error and receiver FIFO overflow error
- Both Inverse and Direct conventions
- Re-transmission of byte upon Smart Card NACK request with programmable threshold of re-transmissions
- Auto detection of Initial Character in receiver and setting of data format, inverse or direct
- NACK detection in receiver
- Independent timers to measure character wait time, block wait time and block guard time
- Two general purpose counters available for use by software application with programmable clock selection for the counters
- DMA support is available to transfer data to/from FIFOs. Programmable option is available to select interrupt or DMA feature
- Programmable Pre-scaler generates the desired frequency for Card Clock and Baud Rate Divisor generates the internal ETU clocks for transmitter and receiver for any F/D ratio
- Deep sleep wake-up via Smart Card presence detect interrupt
- Manual control of all Smart Card interface signals
- Automatic power down of port logic on Smart Card presence detect
- 8-bit LRC and 16-bit CRC generation for bytes from the transmitter and incoming message checksum for the receiver

15 Watchdog

Table 9 lists the watchdog comparison.

Table 9. Watchdog comparison

Items for comparison	i.MX RT1060	i.MX RT1170
Watchdog	2	2
RTWDOG	1	2
External Watchdog Monitor (EWM)	1	1

16 Analog

RT1170 does not contain Touch Screen Controller (TSC).

The ADC peripherals for RT1170 are redesigned LPADC and the block diagram structure is completely different from that of the i.MX RT1060. For details, see *i.MX RT1170 Processor Reference Manual* (document IMXRT1170RM).

Table 10 lists the feature comparison.

Table 10. ADC for i.MX RT1060 and i.MX RT1170

Items for comparison	i.MX RT1060	i.MX RT1170
Max sampling rate	1 MS/s	4.2 MS/s
External analog inputs	16	20
Differential operation with 13-bit resolution	—	√
Result data FIFO supported	—	√
Command buffers	—	15
Channel scaling	—	√

17 Boot

Table 11 lists differences related to system boot between the RT1060 and the RT1170.

Table 11. System boot differences between RT1060 and RT1170

Feature	Decryption	i.MX RT1060	i.MX RT1170
Boot Device	• Serial NOR/NAND • Raw NAND • SD/MMC • 1-bit SPI NOR/EEPROM	Supported	Supported
	• Parallel NOR	Supported	Unsupported
Serial Downloader	Protocol	sdphost	blhost
	• USB-HID	Supported	Supported

Table continues on the next page...

Table 11. System boot differences between RT1060 and RT1170 (continued)

Feature	Decryption	i.MX RT1060	i.MX RT1170
	• UART		
Boot Core	N/A	CM7	CM7/CM4
External RAM destination	• DCD	Supported	Supported
	• XMCD	Unsupported	Supported
Internal RAM ECC	N/A	Unsupported	Supported

18 Security

Table 12 lists differences related to the security between RT1060 and RT1170.

Table 12. Security differences between RT1060 and RT1170

Feature	Decryption	i.MX RT1060	i.MX RT1170
Secure Boot	Authenticated & Encrypted boot	• Supported	• Supported
	Signature Format	• CMS PKCS#1	• CMS PKCS#1
	Public Key Type	• RSA public keys (1024-bit, 2048-bit, 3072-bit and 4096-bit)	• RSA public keys (1024-bit, 2048-bit, 3072-bit and 4096-bit) • ECC (P256/P384/P-521)
	Certificate Format	• X.509v3 certificates	• X.509v3 certificates
	Encrypted XIP	• BEE — AES-128 ECB and CTR — Decrypt cypher context of FlexSPI	• OTFAD1/2 — CTR-AES (128 bit) — Decrypt cypher context of FlexSPI • IEE — XTS-AES 256, 512 bit — CTR-AES 128, 256 bit — RAM encryption/decryption — FlexSPI decryption only
Crypto Engine	Hash Algorithm Engine	• DCP — SHA-1, SHA-256	• CAAM — SHA-1, SHA-2 224/256/384/512 — MD5 — HMAC

Table continues on the next page...

Table 12. Security differences between RT1060 and RT1170 (continued)

Feature	Decryption	i.MX RT1060	i.MX RT1170

	Symmetric Algorithm Engines	• DCP
		  — AES-128 (ECB and CBC modes)
			• CAAM
			  — AES 128, 192, 256 with baseline modes (additional modes include GCM, CMAC)
			  — 3DES/DES

	Asymmetric Algorithm Engine	• DCP
		  — Unsupported
			• CAAM
			  — RSA (up to 4096 bits)
			  — ECDSA (up to 521)
			  — ECDH
			  — Scalar-number Arithmetic
			  — ECC point Arithmetic

	RNG	• SA-TRNG
		  — Entropy source
			• CAAM
			  — RNG4 seeded by TRNG

Key management	Key Mangement	• OCOTP
		  — OTPMK
		  — SW_GP2
			• OCOTP
			  — OTPMK
			  — USER_KEY1/2/3/4/5
			• PUF

Always-on Domain	Secure Non-Volatile Storage (SNVS)	• Secure Real-time Clock (SRTC) • Zero Master Key (ZMK 128 bits) • Digital Low-Voltage Detector • Power glitch detector	• Secure Real-time Clock (SRTC) • Zero Master Key (ZMK 256 bits) • Digital Low-Voltage Detector • Power glitch detector • 4 KB secure retention RAM • Provides a 1 K bit register protected by tamper • Voltage, temperature and Frequency Tamper detector (RT1173 only) • 10 external Tamper PINs (RT1173 only)
Secure Debug	Challenge-response mechanism	• SJC (56 bit response)	• JTAGC (128 bit response)
Others	Access Protection	• CSU	• RDC • xRDC • IEE_APC

Table continues on the next page...

Table 12. Security differences between RT1060 and RT1170 (continued)

Feature	Decryption	i.MX RT1060	i.MX RT1170
	Manufacturing Protection (MP)	• Unsupported	• Supported

For tamper feature application, see *How to use Tamper Function* (document AN13078).

19 Software migration consideration

For software migration, similar with i.MX RT1060, i.MX RT1170 SW ecosystem is based on MCUXpresso SDK/IDE/Tools, as listed in Table 13.

Table 13. SW ecosystem comparison

Items for comparison	i.MX RT1060	i.MX RT1170
MCUXpresso SDK	√	√
MCUXpresso IDE	√	√
MCUXpresso Config Tools	√	√
MCUXpresso Secure Provisioning Tools	√	√
IAR	√	√
Keil	√	√
GCC	√	√

For the software-related silicon features, such as, clock, power mode, new IP on i.MX RT1170, users need to port the codes or re-design on the i.MX RT1170 platform.

Codes related with the same IP feature on both i.MX RT1170 and i.MX RT1060 can be reused. Differences due to different SDK version should be considered.

20 References

- *i.MX RT1170 Processor Reference Manual* (document IMXRT1170RM)
- *i.MX RT1170 Crossover Processors Data Sheet for Consumer Products* (document IMXRT1170CEC)

21 Revision history

Table 14. Revision history

Rev.	Date	Description
0	December 30, 2020	Initial release
1	February 18, 2021	Updated RT1050/60 with RT1060

arm