AN12350

LPC802 Dual IO Power Supply and Level Shift

Rev. 0 — 20 February, 2019 Application Note

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1 Introduction

LPC802(TSSOP20) and LPC804(TSSOP24) come with a new feature, called dual I/O power chip. The feature makes the chip have two power domain: VDDio and VDD. The pins on one side of the package are supplied by VDDIO and the pins on the other side are supplied by VDD. This feature gives different voltages to VDD and VDDIO, and allows the device to level shift signals from one off-chip voltage domain to another.

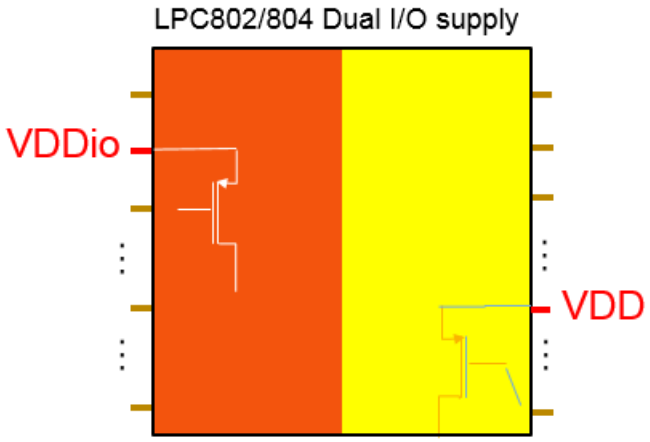

Figure 1. LPC802/804 Dual I/O supply function

Customer can select up to two pins in one voltage domain: In0, In1, and two pins in another voltage domain: Out0, Out1. Use the switch matrix to route them: In0 to Out0, In1 to Out1. It is possible that one signal on pin In(s) can directly go to pins Out(x) with voltage level shifted while do not need any firmware intervening. The only limitation is need for the customer defined Input and Output direction.

1.1 Pin characteristic

The dual power supply feature only applied to specific parts:

LPC802M011JDH20

LPC804M111JDH24

The pin characteristics need alignment with relative power supply.

For pins on VDDio side:

V_O	output voltage	output active		0	-	V_{DDIO}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DDIO}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DDIO}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		V_{DDIO} –0.4	-	-	V
		I_{OH} = 3 mA; 1.71 V <= V_{DD} < 2.5 V		V_{DDIO}– 0.5	-	-	V

Figure 2. Pin spec for VDDio side

For pins on VDD side:

V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	0.4	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA; 2.5 V <= V_{DD} <= 3.6 V		V_{DD} – 0.4	-	-	V
		I_{OH} = 3 mA; 1.71 V <= V_{DD} < 2.5 V		V_{DD} – 0.5	-	-	V

Figure 3. Pin spec for VDD side

ADC power domain connects VDD domain. For ADC operation, the VDD voltage must be above 2.5 V.

1.2 Pin comparison

Some functions assigned to pins are different between single power supply (SS) chip and dual power supply (DS) chip, See Figure 4. on page 2.

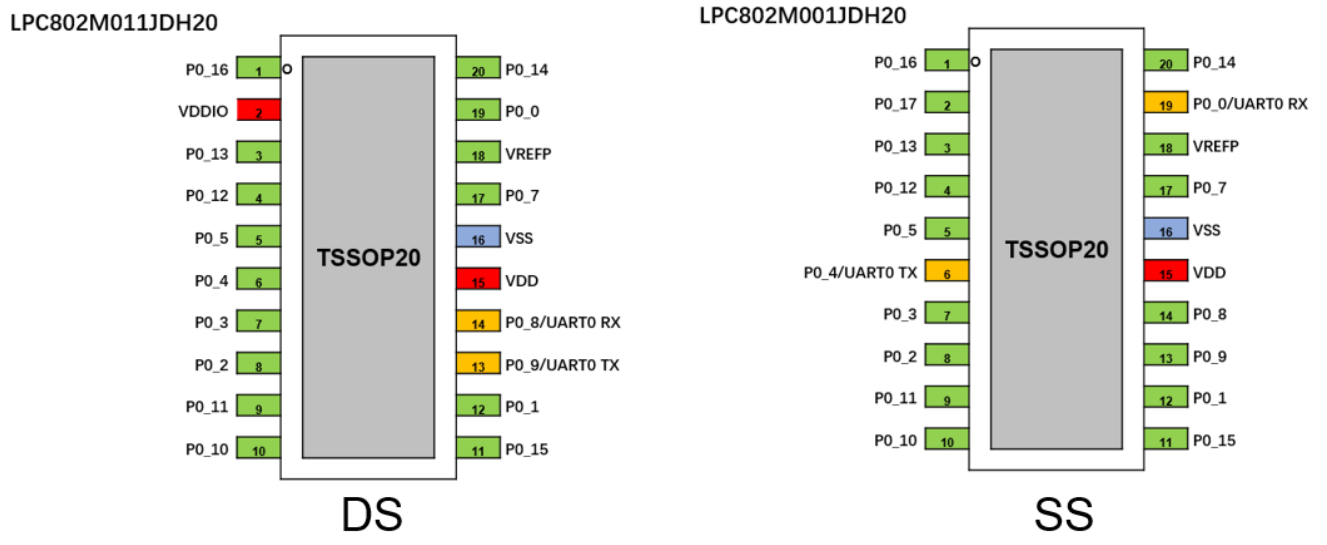

Figure 4. Pin comparison between SS and DS chip

In DS chip, the pin2 is used as VDDio, while in SS chip it is used as PIO0_17 (pins marked in red color).

DS / SS chip has different pin assignment for ISP USART (pins marked in yellow color).

2 Demo for level shift

2.1 Demo introduction

To communicate between the applications working on different work voltage, there is a need to add a level shift device between them. In this demo, LPC802 is used to level shift signals between two voltage applications, VDD side GPIO (PIO0_14) connected to a 3.3 v application, and VDDio side GPIO (PIO0_11) connected to a 1.8 v application. Before starting the communication, LPC802 uses switch matrix to configure PIO0_14 as level shift input0 - In0, PIO0_11 as level shift output0 - Out0. After configuration, any 3.3 v logic level signal input on In0 automatically converts to Out0 with logic level changed to 1.8 v without software intervening.

Demo used SWM register PINASSIGN6 to configurate PIO0_14 as level shift In0, PIO0_11 as level shift Out0.

To demonstrate easily by one board, the demo uses GPIO0_9 to output a 3.3 v square wave, then connect PIO0_9 to PIO0_14 (In1), see Figure 5. on page 3.

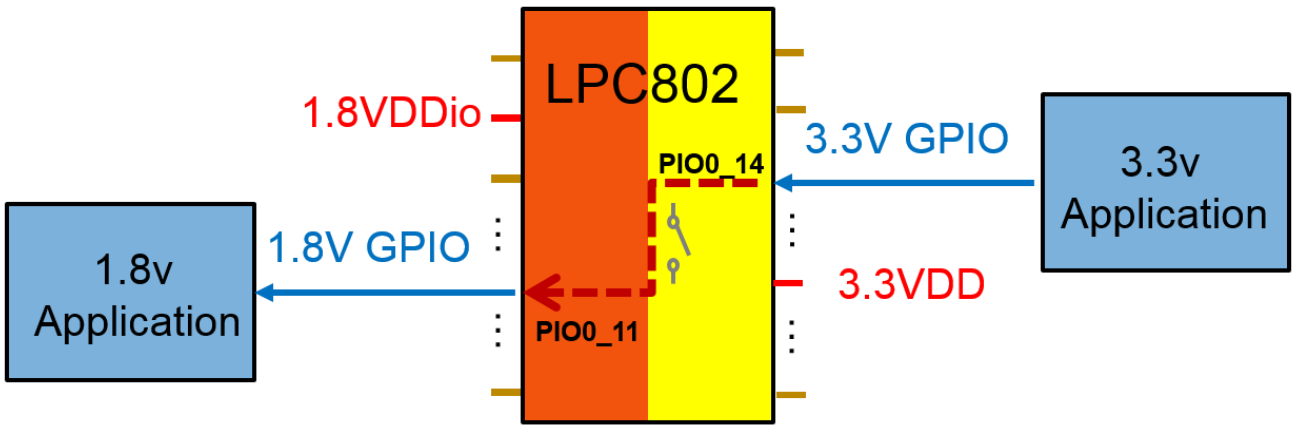

Figure 5. LPC802 level shift demo

2.2 Demo hardware

2.2.1 Board

LPCXpresso802 board (OM40000).

2.2.2 Debugger

Integrated on-board debugger providing a CMSIS-DAP interface

2.2.3 Board setup

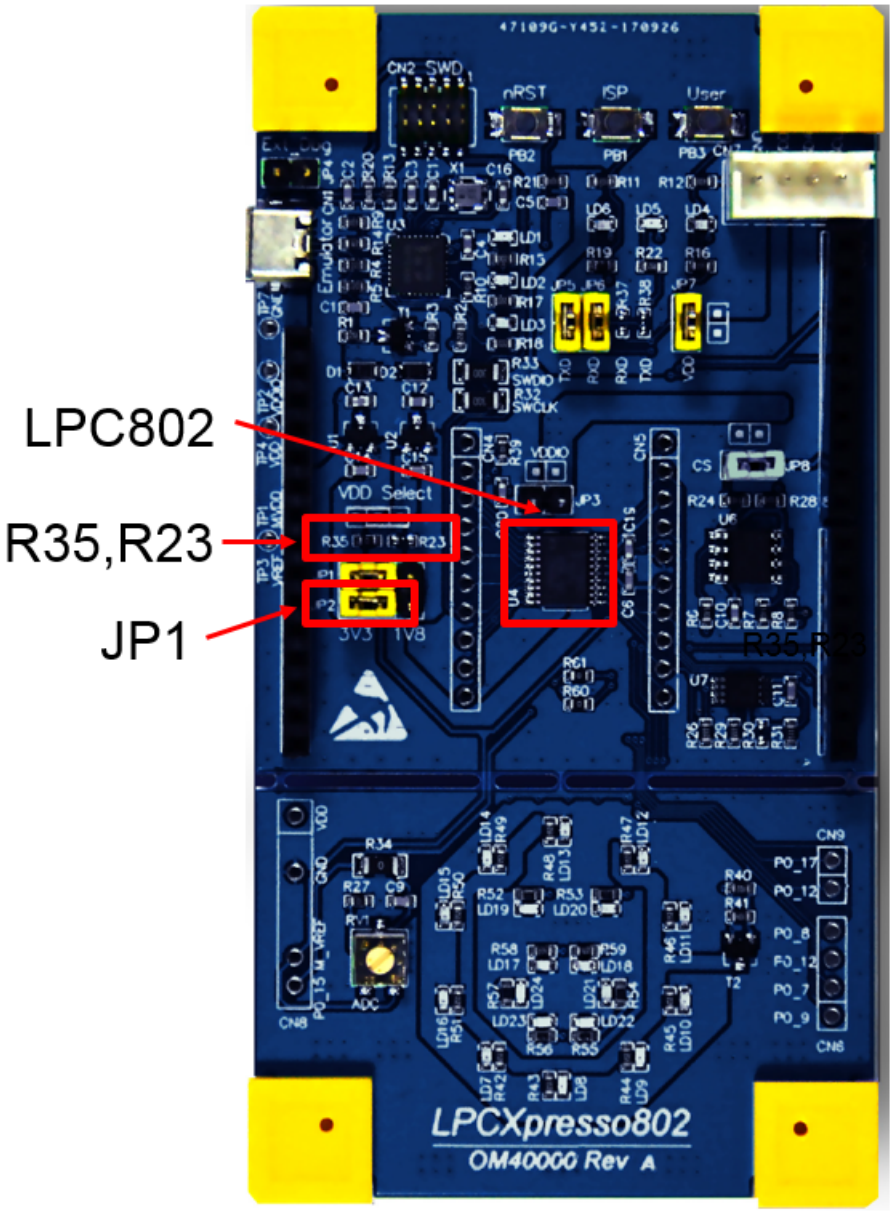

Figure 6. Board setup

- JP1 must be connected to 3.3 V side, else, UART does not output correct information.
- Replace LPC802M001JDH20 (SS chip) with LPC802M011JDH20 (DS chip), make dual I/O power supply feature available.
- Remove R35, Put R23(0 ohm), it makes VDDIO = 1.8 V

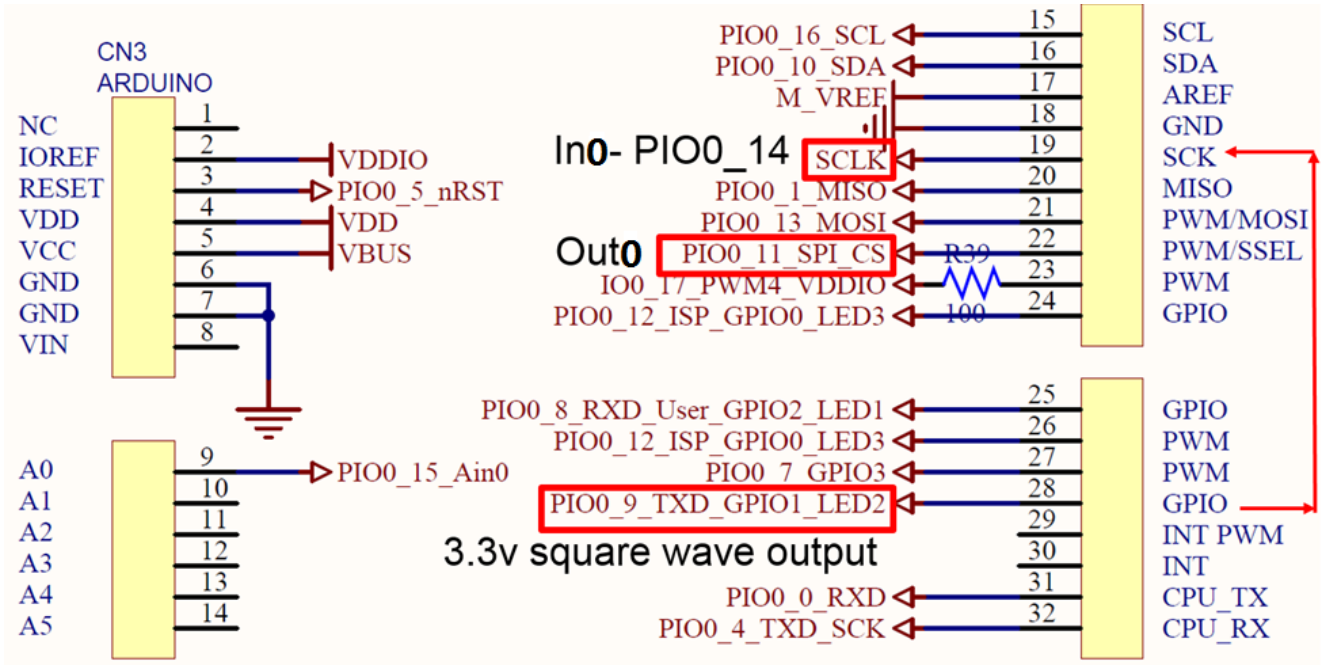

Figure 7. Connect relative pins

Connect PIO0_9 to PIO0_14 on the arduino port CN3.

2.3 Demo software

Development IDE:

- IAR embedded Workbench 8.22.2

- Keil MDK 5.24a

- MCUXpresso10.2.0

2.4 Demonstration

2.4.1 Demo steps

1. Connect a micro USB cable between the PC host and the CMSIS DAP port, CN1 on the LPCXpresso802 board.
2. Open a serial terminal in PC (for example Tera Term) with following settings:
   - 9600 baud-rate
   - 8 data bits
   - No parity
   - One stop-bit
   - No flow controls
3. Compile and download the code to the target board.

4. Launch the debugger in your IDE to begin running the project.
5. Monitor the information on the debug console.
6. Use oscilloscope to watch the 3.3 v input square wave on pin PIO0_14_SCLK and 1.8 v output square wave on pin PIO0_11.

2.4.2 Demo result

After running Demo, serial terminal in PC prints information as Figure 8. on page 6:

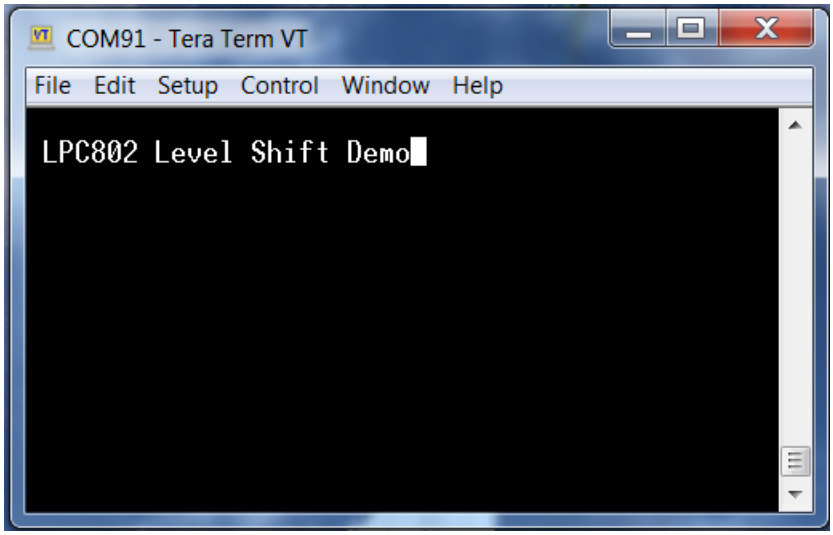

Figure 8. Serial terminal information

Use Oscilloscope to watch the PIO0_14_SCLK (VDD Domain, Level Shift input) and PIO0_11 (VDDIO domain, Level Shift output), You can see square wave level shift from 3.3 v to 1.8 v.

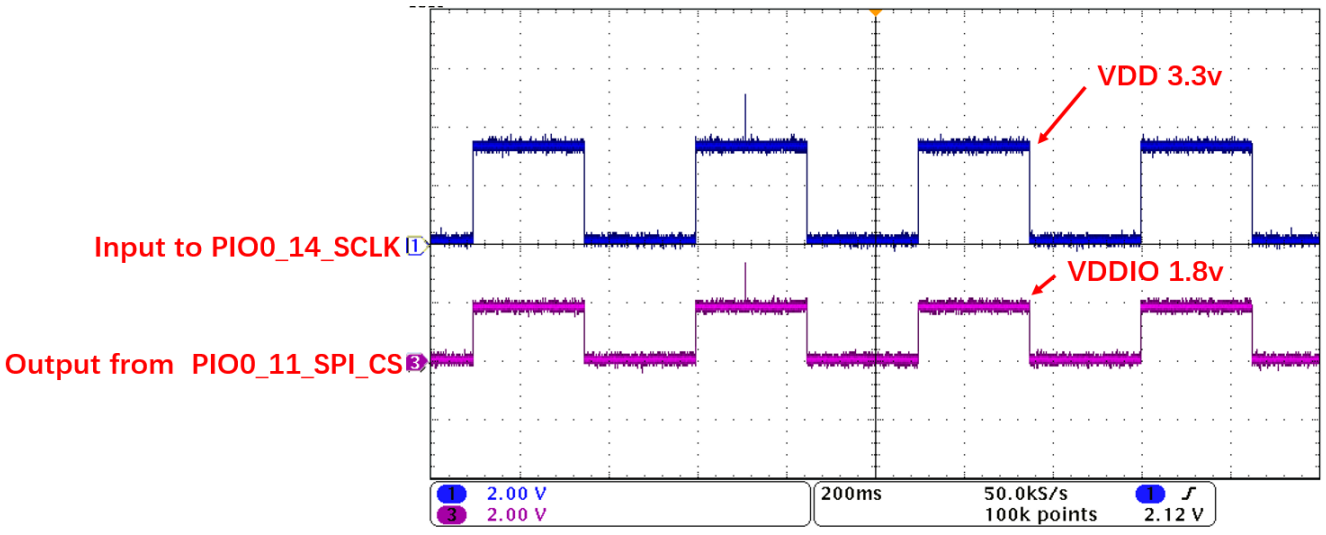

Figure 9. Level shifted square wave

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