Document Number: K32L3A
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K32L3A

72 MHz Arm® Cortex®-M0+/M4F Dual Core Microcontroller with up to 1280 KB Flash and 384 KB SRAM

K32L3A60VPJ1AT

The K32L3A family of devices is an ultra-low-power, dual core solution ideal for applications that require a high performance Cortex-M4F processor to run the application and an efficient Cortex-M0+ to run low power operations such as sensor data collection and perform low level operations that don't need the full power of the M4 core.

176 VFBGA
9 x 9 x 1 mm Pitch 0.5 mm

Core Processor

- Arm Cortex-M4F core up to 72 MHz (high-speed run up to 72 MHz) for application code
- Arm Cortex-M0+ core up to 72 MHz (high-speed run up to 72 MHz) for low power operations

Memories

- 1.25 MB program flash memory, 1 MB on the M4F domain and 256 KB on the M0+ domain
- 384 KB SRAM, 256 KB on the M4F domain and 128 KB on the M0+ domain
- 48 KB ROM with built-in bootloader
- 32 B system register file and 32 B RTC register file
- External bus interface (FlexBUS) for off-chip memory expansion

Clocks

- Low-Power Frequency-Locked Loop (LPFLL)
  - Range 1: 48 MHz
  - Range 2: 72 MHz
- Internal Resistance-Capacitance Oscillators (IRCs)
  - Fast-Speed IRC (48, 52, 56, 60 MHz)
  - Slow-Speed IRC (8 MHz or 2 MHz)
  - Low Power Oscillator (LPO - 1 kHz)
- Real Time Clock Oscillator (RTCOSC)
- System Clock Generation

System

- Dual Direct Memory Access (DMA) controllers with asynchronous capability
  - M4F: 16 channels, 64 inputs per channel
  - M0+: 8 channels, 32 inputs per channel

Timers

- 2 x 6 ch., 2 x 2 ch. Timer PWM Modules (TPM)
- 2 x 4 ch. Low Power Programmable Interrupt Timer (LPIT)
- 3 Low Power Timer (LPTMR)
- Real Time Clock (RTC)
- One 56-bit Time stamp

Security and Integrity

- 80-bit unique identification number per chip
- Advanced Flash security and access control
- 16-bit or 32-bit Hardware CRC with programmable generator polynomial
- Low-power Cryptographic Acceleration Unit (CAU3) supporting AES128/196/256, DES/3DES, SHA 256, RSA and ECC PK-256/Curve25519
- True Random Number Generator
- Up to 4 active anti-tamper detection pins

Analog

- 1 x 12-bit single ended low-power ADC
- 2 x Low power comparator (LPCMP) each containing a 6-bit DAC and programmable reference input
- 1 x 12-bit low power digital-to-analog converter (LPDAC)
- 1 x 1.2V/2.1V dual-range VREF

Peripherals

- 1 x Universal Serial Bus (USB) 2.0 Full Speed (FS) controller with integrated hardware transceiver, 5 V regulator and 2 KB USB RAM

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

- Two internal Watchdog and one external Watchdog Monitor
- Low-leakage wakeup unit
- JTAG and Serial Wire Debug, version 2.0, programming and debug interface with multi-drop capability
- Trace Features for M4F
  - Cross Trigger Interface
  - Embedded Trace Macrocell
  - Trace Port Interface Unit
- Trace Features for M0+
  - Cross Trigger Interface
  - Micro Trace Buffer
  - Breakpoint and Watchpoint Unit
- Nested Vectored Interrupt Controller
- Memory Protection Unit
- Extended Resource Domain Controller

Power Management

- Bypass mode: 1.71 V to 3.6 V
- Buck DC-DC converter: 2.1 V to 3.6 V
- Core voltage bypass: 1.14 V to 1.45 V direct supply to core, bypassing internal regulator
- Independent VDDIO1 and VDDIO2 supply: 1.71 V to 3.6 V
- Independent VBAT(RTC): 1.71 V to 3.6 V

- 1 x 32 ch. FlexIO supporting emulation of UART, I2C, SPI, I2S, Camera IF, LCD RGB, PWM/Waveform generation
- 4 x low power UART (LPUART)
- 4 x low power I2C (LPI2C) modules supporting up to 1 Mbps
- 4 x 16-bit low power SPI (LPSPI) supporting up to 24 Mbps
- 1 x EMVSIM module supporting supporting ISO-7816 protocol
- 1 x Serial Audio Interface (SAI) with support for I2S and AC'97
- 1 x Secure Digital Hardware Controller (uSDHC)

I/O

- 104 General-purpose input/output pins (GPIO)

Packages

- 176 VFBGA 9mm x 9mm x 0.86mm, 0.5mm pitch, -40 °C to 105 °C

Related resources

Type	Description
Selector Guide	The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.
Package drawing	Package dimensions are provided in package drawings.

Table of Contents

1 Ordering information

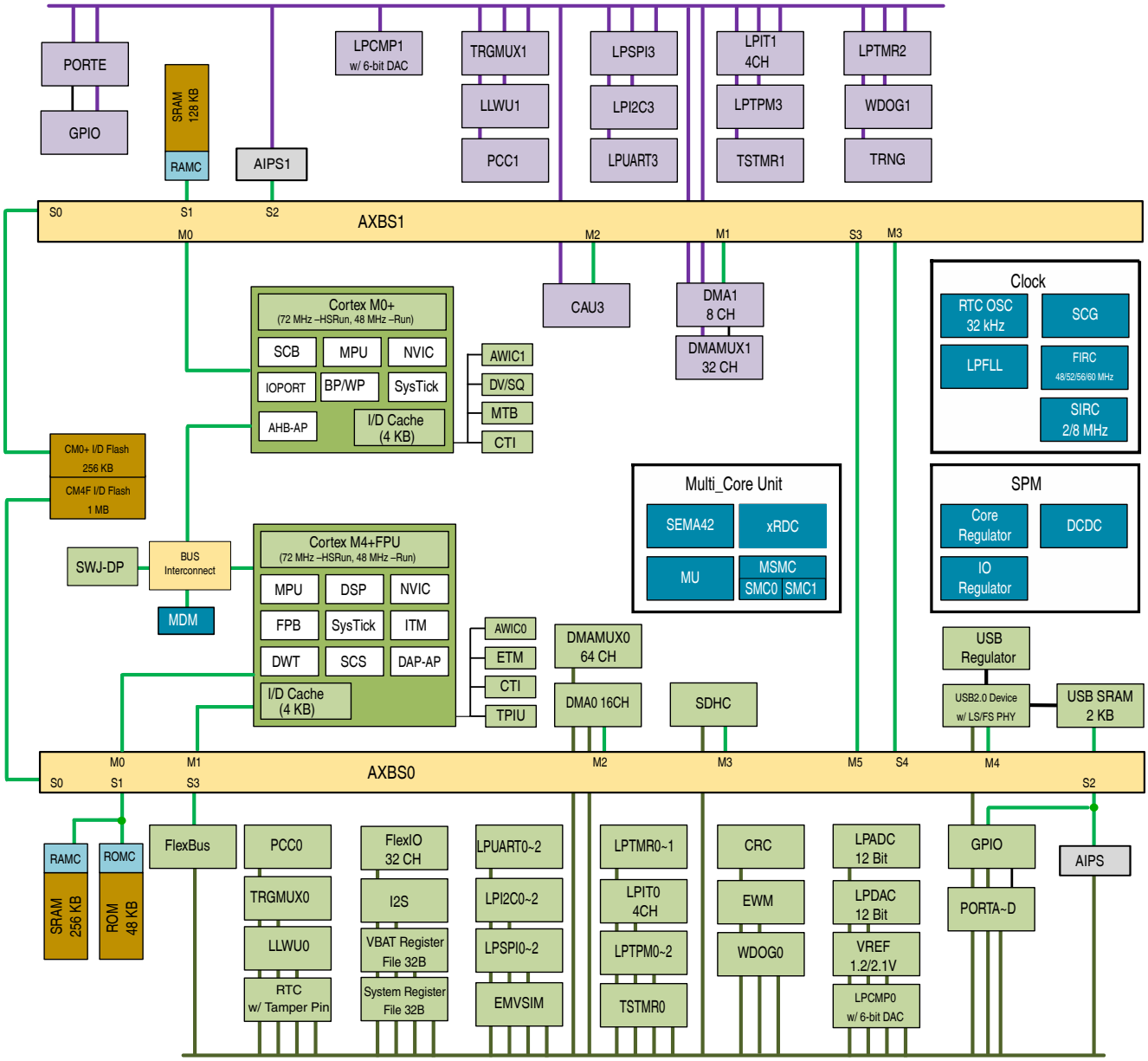
The following table summarizes the part numbers of the devices covered by this document.

Table 1. Ordering information

Product		Memory		Package	
Part Number	Marking	Flash (MB)	SRAM (KB)	Pin Count	Package
K32L3A60VPJ1AT	K32L3A60VPJ1AT	1.25	384	176	VFBGA

2 Overview

The following figure shows the system diagram of this device



Note: When a core needs access the other AXBS domain resources, the corresponding MUx_CCR[CLKE] bit must be set. AXBS keeps active even if another core enters low power mode (and CPO).

Figure 1. System diagram

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously for AXBS1 and up to six for AXBS0, while providing arbitration among the bus masters when they access the same slave.

2.1 System features

The following sections describe the high-level system features.

2.1.1 Arm Cortex-M0+ core

The enhanced Arm Cortex M0+ is the member of the Cortex-M series of processors targeting microcontroller cores focused on very cost sensitive, low power applications. It has a single 32-bit AMBA AHB-Lite interface and includes an NVIC component. It also has hardware debug functionality including support for simple program trace capability. The processor supports the Arm v6-M instruction set (Thumb) architecture including all but three 16-bit Thumb opcodes (52 total) plus seven 32-bit instructions. It is upward compatible with other Cortex-M profile processors.

This device supports hardware divider (MMDVSQ) when CM0+ core is working.

2.1.2 Arm Cortex-M4 core

The Cortex M4 processor is based on the Armv7 Architecture and Thumb®-2 ISA and is upward compatible with the Cortex M3, Cortex M1, and Cortex M0 architectures. Cortex M4 improvements include an Armv7 Thumb-2 DSP (ported from the Armv7-A/R profile architectures) providing 32-bit instructions with SIMD (single instruction multiple data) DSP style multiply-accumulates and saturating arithmetic.

2.1.3 NVIC

The Armv7-M exception model and nested-vectored interrupt controller (NVIC) implement a relocatable vector table supporting many external interrupts, a single non-maskable interrupt (NMI), and priority levels.

The NVIC replaces shadow registers with equivalent system and simplified programmability. The NVIC contains the address of the function to execute for a particular handler. The address is fetched via the instruction port allowing parallel register stacking and look-up. The first sixteen entries are allocated to Arm internal sources with the others mapping to MCU-defined interrupts.

2.1.4 AWIC

The primary function of the Asynchronous Wake-up Interrupt Controller (AWIC) is to detect asynchronous wake-up events in stop modes and signal to clock control logic to resume system clocking. After clock restart, the NVIC observes the pending interrupt and performs the normal interrupt or event processing.

The device uses the following internal and external inputs to the AWIC module. AWIC0 is AWIC in CM4F domain while AWIC1 is AWIC in CM0+ domain.

Table 2. AWIC0 Stop and VLPS wakeup sources

Wake-up source	Description
System resets	All available system resets sources are describted in SMC0 under MSMC chapter
SPM	All available interrupt in SPM, such as low/high voltage detect interrupt, low voltage detect/warnning interrupt, and etc.
Pin	PTA, PTB, PTC, PTD, PTE pin interrupts
LPUART0~3	Functional when using clock source which is active in Stop and VLPS modes
LPI2C0~3	Address match wakeup
LPSPI0~3	Slave mode interrupt
I2S	Functional when using an external bit clock or external master clock
EMVSIM	Any enabled interrupt can be a source as long as the module remains clocked.
USB Controller	Wakeup
Secure Digital Hardware Controller (SDHC)	Wakeup
FlexIO	Functional when using clock source which is active in Stop and VLPS modes
LPTMR0~2	Functional when using clock source which is active in Stop, VLPS and LLS/VLLS modes
TPM0~3	Functional when using clock source which is active in Stop and VLPS modes
RTC	Functional in Stop, VLPS, LLS and VLLSx modes
LPIT0/1	Any enabled interrupt can be a source as long as the module remains clocked.
Tamper detect	Interrupt
NMI	NMI is routed to CM4F or CM0+ automatically, only boot core has NMI
LPCMP0/1	Interrupt in normal or trigger mode
LPDAC	Any enabled interrupt can be a source as long as the module remains clocked.

Table continues on the next page...

Table 2. AWIC0 Stop and VLPS wakeup sources (continued)

Wake-up source	Description
LPADC	The LPADC is functional when using internal clock source
LLWU0	Any enabled interrupt can be a source as long as the module remains clocked.
MUA	Any enabled interrupt can be a source as long as the module remains clocked.
WDOG0	Watchdog0 Interrupt

Table 3. AWIC1 Stop and VLPS wakeup sources

Wake-up source	Description
System resets	All available system resets sources are describted in SMC1 under MSMC chapter
PortE	PTE pin interrupts
LPUART3	Functional when using clock source which is active in Stop and VLPS modes
LPI2C03	Address match wakeup
LPSPI3	Any enabled interrupt can be a source as long as the module remains clocked.
LPTMR2	Functional when using clock source which is active in Stop, VLPS and LLS/VLLS modes
TPM3	Functional when using clock source which is active in Stop and VLPS modes
RTC	Functional in Stop,VLPS,LLS and VLLSx modes
LPIT1	Any enabled interrupt can be a source as long as the module remains clocked.
NMI	NMI is routed to CM4F or CM0+ automatically, only boot core has NMI
LPCMP1	Interrupt in normal or trigger mode
TRNG	TRNG has no stop wakeup capability
LLWU1	Any enabled interrupt can be a source as long as the module remains clocked.
MUB	Any enabled interrupt can be a source as long as the module remains clocked.
WDOG1	Watchdog1 Interrupt
INTMUX0~7	All other wakeup sources availabe in AWIC0 can be selected through INTMUXn. Please refer to the INTMUXn description.

2.1.5 Memory

This device has the following features:

- 384 KB of embedded RAM accessible (read/write) at CPU clock speed with 0 wait states.
- 4 KB of embedded RAM used for flash programming acceleration RAM
- The non-volatile memory is divided into two arrays
  - 2 blocks of program flash, providing 1 MB consisting of 4 KB sectors for CM4
  - 1 block of program flash, providing 256 KB consisting of 2 KB sectors for CM0+

  The primary program flash memory contains an IFR space that stores default protection settings and security information.

  The protection setting can protect 64 regions of the primary program flash memory and 16 regions of the secondary program flash memory from unintended erase or program operations.

  The security circuitry prevents unauthorized access to RAM or flash contents from debug port.

- System register file

  This device contains a 32-byte register file that is powered in all power modes.

  Also, it retains contents during low power modes and is reset only during a power-on reset.

- VBAT register file

  This device includes a 32-byte register file. The register file is powered by the VBAT domain and is powered in all modes as long as power is applied to the VBAT supply.

  The VBAT register file is only reset during the VBAT Power-on Reset (PORVBAT) sequence.

2.1.6 Reset and boot

The following table lists all the reset sources supported by this device.

NOTE

In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the

specific module is not reset by the corresponding Reset source.

Table 4. Reset source

Reset sources	Descriptions	Modules							
		SPM	SIM	MSMC	LLWU	Reset pin is negated	RTC[1]	LPTMR	Others
POR reset	Power-on reset (POR)	Y	Y	Y	Y	Y	N	Y	Y
System reset	Low leakage wakeup (LLWU) reset	N[2]	Y[3]	N	N	Y[4]	N	N	Y[5]
	External pin reset (RESET_b)	N[2]	Y[3]	Y[6]	Y	Y	N	N	Y
	Computer operating properly (COP) watchdog reset	N[2]	Y[3]	Y[6]	Y	Y	N	N	Y
	Stop mode acknowledge error (SACKERR)	N[2]	Y[3]	Y[6]	Y	Y	N	N	Y
	Software reset (SW)	N[2]	Y[3]	Y[6]	Y	Y	N	N	Y
	Lockup reset (LOCKUP)	N[2]	Y[3]	Y[6]	Y	Y	N	N	Y
	MDM DAP system reset	N[2]	Y[3]	Y[6]	Y	Y	N	N	Y
Debug reset	Debug reset	N	Y[3]	Y[6]	Y	Y	N	N	Y

1. The VBAT POR asserts on a VBAT POR reset source. It affects only the modules withinthe VBAT power domain: RTC and VBAT Register File. These modules are not affected by the other reset types.
2. Except SPM_CORESC[ACKISO], SPM_CORESC[VSEL] and SPM_CORESC[VSEL_OFFSET]
3. The SIM_SDID, SIM_RREPCR1, SIM_RREPCR2, SIM_RREPSR1, SIM_RREPSR2, SIM_FCFG2, SIM_UIDH, SIM_UIDM, SIM_UIDL, registers are not affected by the reset to exit from VLLS2 or VLLS3 modes.
4. Only if RESET_b is used to wake from VLLS mode.
5. The FTFE, LPCAC and LPLMEM modules cannot be reset when chip is waken up from VLLS2 or VLLS3 modes by LLWU.
6. Except SMCx_PMCTRL and SMCx_PMSTAT of the MSMC.

The CM0+ core adds support for a programmable Vector Table Offset Register (VTOR) to relocate the exception vector table after reset. This device supports booting from:

- internal flash
- ROM

The Flash Option (FOPT) register in the Flash Memory module (FTFE_FOPT) allows the user to customize the operation of the MCU at boot time. The register contains read-only bits that are loaded from the NVM's option byte in the IFR spaces. Below is boot flow chart for this device.

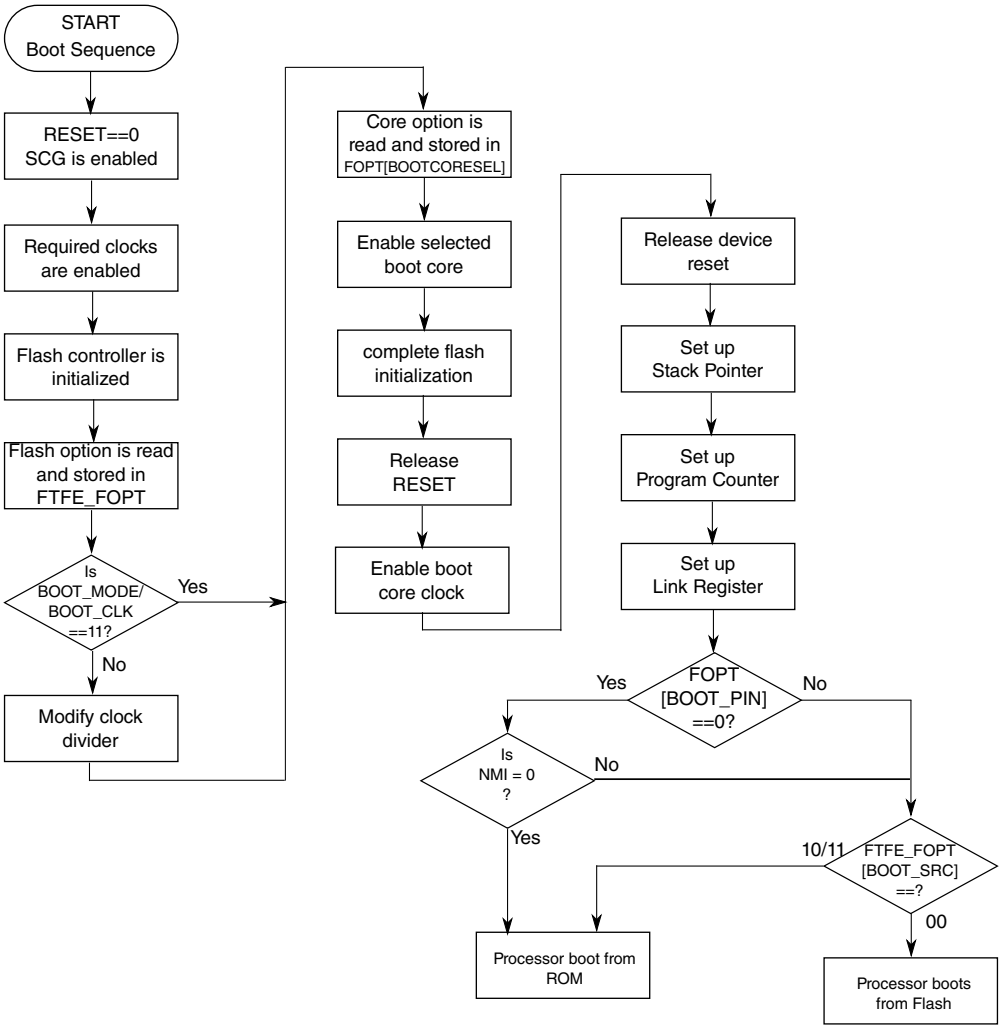


Figure 2. Boot sequence

Blank chips default to boot from ROM and remap the vector table to ROM base address, otherwise, it remaps to flash address.

If booting from ROM, the device executes in boot loader mode.

2.1.7 ROM bootloader

The Kinetis bootloader is the program residing in the on-chip read-only memory (ROM) of a Kinetis microcontroller device. There is hardware logic in place at boot time that either starts execution of an embedded image available on the internal flash memory, or starts the execution of the Kinetis Bootloader from on-chip ROM.

Features supported by the Kinetis Bootloader in Kinetis ROM:

- Supports USB, LPI2C, LPSPI, and LPUART peripheral interfaces

- Automatic detection of the active peripheral
- Ability to disable any peripheral
- LPUART peripheral implements autobaud
- Common packet-based protocol for all peripherals
- Packet error detection and retransmission
- Flash-resident configuration options
- Fully supports internal flash security, including ability to mass erase or unlock security via the backdoor key
- Protection of RAM used by the bootloader while it is running
- Provides command to read properties of the device, such as flash and RAM size
- Multiple options for executing the bootloader either at system start-up or under application control at runtime
- Supports internal flash
- Supports encrypted image download
- ROM boots from either M4 (Default) or M0+ by configuring to FOPT IFR (record Index 0x84)

2.1.8 Clock options

This chip provides a wide range of sources to generate the internal clocks. These sources include internal reference clock (IRC) oscillators, external oscillators, external clock sources, ceramic resonators, and frequency-locked loop (FLL). These sources can be configured to provide the required performance and optimize the power consumption.

The IRC oscillators include the fast internal reference clock (FIRC) oscillator, the slow internal reference clock (SIRC) oscillator, and the low power oscillator (LPO).

The fast internal resistor capacitor (FIRC) oscillator generates a clock ranging between 48 MHz and 60 MHz.

The slow internal resistor capacitor (SIRC) oscillator generates clock at either 8 MHz or 2 MHz. It can serve as the low power, low speed system clock under very low power run (VLPR) mode or very low power wait (VLPW) mode. It can also be provided as clock source for other on-chip modules. The SIRC cannot be used in any VLLS modes.

The LPO generates a 1 kHz clock and default to be off in VLLS0 but can be enabled by configuring bits of SPM_CORELPCNFG[LPOEN] and SPM_CORELPCNFG[ALLREFEN].

The frequency-locked loop (FLL) can generate a clock with the frequency of 48 MHz or 72 MHz without the need of a reference (a reference clock may only be needed to trim this clock). The FLL can be used as the system clock or clock source for other on-chip modules.

The RTC oscillator supports low speed crystals (32.768 kHz) and can also support external clock on the EXTAL32 pin for use with the RTC.

For more details on the clock operations and configurations, see Reference Manual.

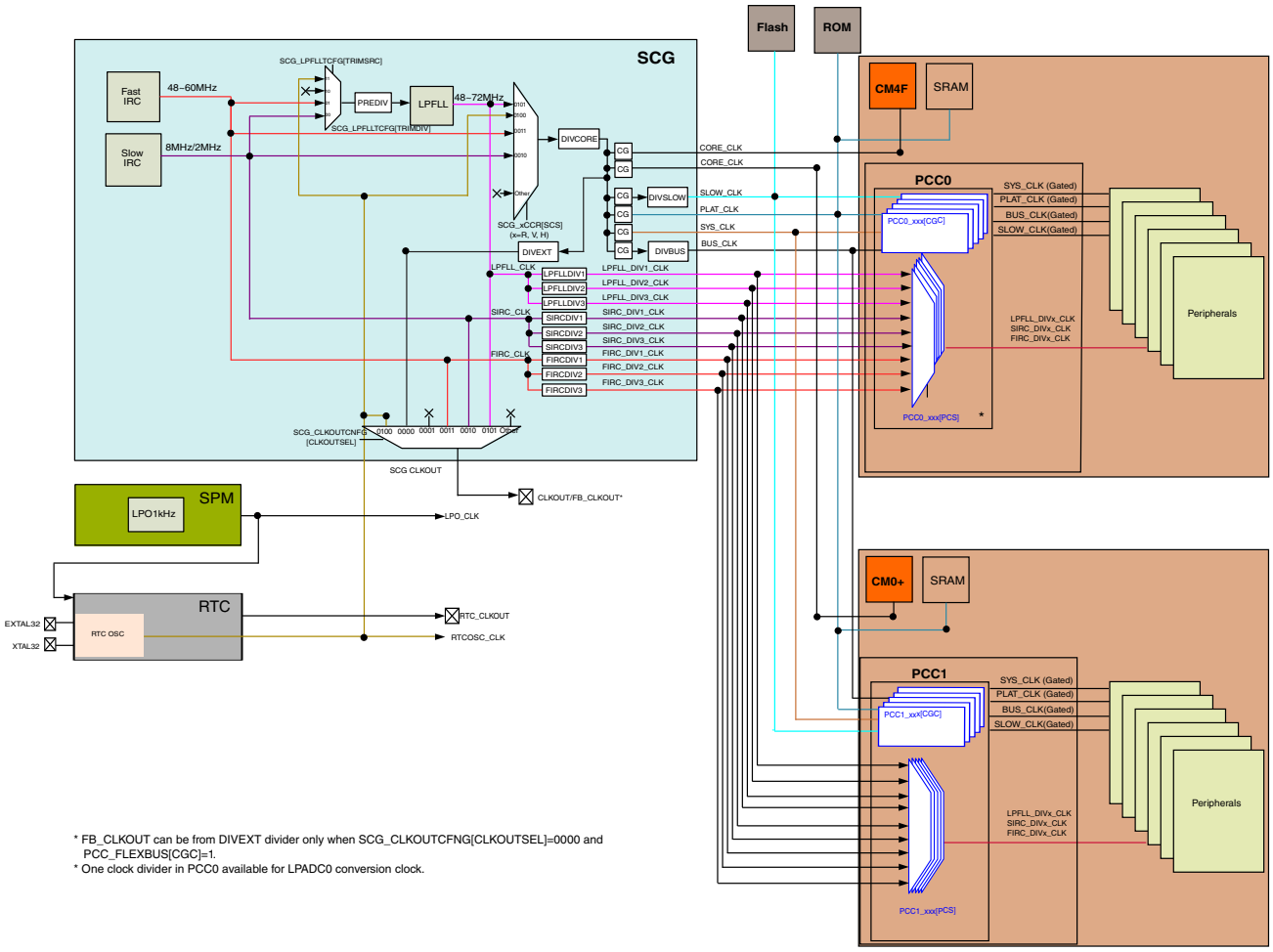


Figure 3. Generic clocking architecture diagram

In order to provide flexibility, many peripherals can select from multiple clock sources for operation. This enables the peripheral to select a clock that will always be available during operation in various operational modes.

The following table summarizes the clocks associated with each module.

Table 5. Clock assignments

Module Name	Bus Interface Clock	PCC Clock Gate	Peripherial Functional Clock	Clock Domain[1]	I/O Interface Clocks
Core Modules					
Arm Cortex-M0+ Core	CORE_CLK	—	—	SCG	—
Arm Cortex-M4 Core	CORE_CLK	—	—	SCG	—
CM0+ TRACE	SYS_CLK	Yes	SYS_CLK	SCG	—
CM4F TRACE	SYS_CLK	Yes	SYS_CLK, SIRC_DIV1_CLK, FIRC_DIV1_CLK, LPFLL_DIV1_CLK	PCC0	TRACE_CLK_OUT
JTAG	NA	—	TCK	—	JTAG_TCLK
SWD	PLAT_CLK	—	SWCK	SCG[2]	SWD_CLK
Platform Modules					
CM0+ Crossbar	PLAT_CLK	—	NA	SCG	—
CM4F Crossbar	PLAT_CLK	—	NA	SCG	—
xRDC	PLAT_CLK	Yes	—	PCC0,PCC1	—
SEMA42	PLAT_CLK	Yes	—	PCC0,PCC1	—
System Modules					
MSMC_SMC0	SLOW_CLK	Yes	—	PCC0	—
MSMC_SMC1	SLOW_CLK	Yes	—	PCC1	—
INTMUX	BUS_CLK		—	SCG	—
DMA0	SYS_CLK	Yes	—	PCC0	—
DMA1	SYS_CLK	Yes	—	PCC1	—
DMA MUX0	BUS CLK	Yes	—	PCC0	—
DMA MUX1	BUS CLK	Yes	—	PCC1	—
EWM	SLOW_CLK	Yes	LPO clock.	PCC0[2]	—
LLWU0	SLOW_CLK	Yes	LPO	SCG[2]	—
LLWU1	SLOW_CLK	Yes	LPO	SCG[2]	—
MU	SLOW_CLK	Yes	—	PCC0,PCC1	—
SPM	SLOW_CLK	Yes	—		—
TRGMUX0	SLOW_CLK	Yes	—	SCG	—
TRGMUX1	SLOW_CLK	Yes	—	SCG	—
WDOG0	SLOW_CLK	Yes	LIRC, or LPO clock.	PCC0[2]	—
WDOG1	SLOW_CLK	Yes	LIRC, or LPO clock.	PCC1[2]	—
Memories					
Flash Controller (FMC)	PLAT_CLK	—	—	SCG	—

Table continues on the next page...

Table 5. Clock assignments (continued)

Module Name	Bus Interface Clock	PCC Clock Gate	Peripherial Functional Clock	Clock Domain[1]	I/O Interface Clocks
Flash Memory (FTFE)	SLOW_CLK	—	—	SCG	—
FlexBus	PLAT_CLK	Yes	—	PCC0[2]	FB_CLKOUT/ CLKOUT
CM4F SRAM	PLAT_CLK	—	PLAT_CLK	SCG	—
CM0+ SRAM	PLAT_CLK	—	PLAT_CLK	SCG	—
Security and Integrity					
CAU3	SYS_CLK	Yes	—	PCC1	—
CRC	BUS_CLK	Yes	—	PCC0	—
TRNG	BUS_CLK	Yes	—	PCC1	—
Timers					
LPIT0	SLOW_CLK	Yes	SIRC_DIV3_CLK, FIRC_DIV3_CLK, LPFLL_DIV3_CLK	PCC0	—
LPIT1	SLOW_CLK	Yes	SIRC_DIV3_CLK, FIRC_DIV3_CLK, LPFLL_DIV3_CLK	PCC1	—
RTC	SLOW_CLK	Yes	RTCOSC, LPO	SCG[2]	RTC_CLKOUT
LPTMR0/1	SLOW_CLK	—	SIRC_DIV3_CLK, LPO, RTCOSC	SCG[2]	—
LPTMR2	SLOW_CLK	—	SIRC_DIV3_CLK, LPO, RTCOSC	SCG[2]	—
LPTPM0~2	BUS_CLK	Yes	SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC0[2]	TPM0~32_CLKIN
LPTPM3	BUS_CLK	Yes	SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC1[2]	TPM3_CLKIN
TSTMR	SLOW_CLK	Auto	SIRC_1MHZ_CLK	SCG	—
Communication Interfaces					
EMVSIM	BUS_CLK	Yes	SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK , RTCOSC	PCC0	EMVSIM_CLK
FlexIO	BUS_CLK	Yes	SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC0	—
LPI2C0~2	BUS_CLK	Yes	SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC0	LPI2C0~2_SCL
LPI2C3	BUS_CLK	Yes	SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC1	LPI2C3_SCL

Table continues on the next page...

Table 5. Clock assignments (continued)

Module Name	Bus Interface Clock	PCC Clock Gate	Peripherial Functional Clock	Clock Domain[1]	I/O Interface Clocks
I2S	BUS_CLK	Yes	SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK, SAI_MCLK	PCC0[3]	SAI_TX_BCLK, SAI_RX_BCLK, SAI_MCLK
uSDHC	SYS_CLK	Yes	SIRC_DIV1_CLK, FIRC_DIV1_CLK, LPFLL_DIV1_CLK, SDHC_DCLK	PCC0	SDHC_DCLK
LPSPI0~2	BUS_CLK	Yes	SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC0	LPSPI0~2_SCK
LPSPI3	BUS_CLK	Yes	SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC1	LPSPI3_SCK
LPUART0~2	BUS_CLK	Yes	SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC0	—
LPUART3	BUS_CLK	Yes	SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC1	—
USB	SYS_CLK	Yes	SIRC_DIV1_CLK, FIRC_DIV1_CLK, LPFLL_DIV1_CLK	PCC0[2]	—
USB SRAM	SIRC_DIV1_CLK, FIRC_DIV1_CLK, LPFLL_DIV1_CLK, SYS_CLK	Yes	—	PCC0[2]	—
Human-Machine Interfaces					
PORTA~D	SLOW_CLK	Yes	SLOW_CLK, LPO	PCC0	—
PORTE	SLOW_CLK	Yes	SLOW_CLK, LPO	PCC1	—
RGPIOA~D	PLAT_CLK	Yes	—	PCC0	—
RGPIOE	PLAT_CLK	Yes	—	PCC1	—
Analog					
LPADC	BUS_CLK	Yes	SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK, LPADC Internal Clock.	PCC0	—
LPCMP0	SLOW_CLK	—	—	SCG	—
LPCMP1	SLOW_CLK	—	—	SCG	—
LPDAC	BUS_CLK	Yes	—	PCC0	—
VREF	SLOW_CLK	Yes	—	PCC0	—

1. PPC0 controls CM4F domain,and PPC1 controls CM0+ domain.
2. It is bus interface clock domain.
3. SAI_MCLK doesn't blong to PCC clock domain.

2.1.9 Security

Security state can be enabled via programming Flash IFR SEC0 (index 0x80). After enabling device security, the SWJ (SWD and JTAG) port cannot access the memory resources of the MCU, and ROM boot loader is also limited to access flash and not allowed to read out flash information via ROM boot loader commands.

Access interface	Secure state	Unsecure operation
SWJ (SWD and JTAG) port	Cannot access memory source by SWD interface	The debugger can write 1 to the System Reset Request field and Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks Unsecure) command
ROM boot loader Interface (LPUART/ LPI2C/LPSPI/USB)	Limit access to the flash, cannot read out flash content	Send “FlashEraseAllUnsecure" command or attempt to unlock flash security using the backdoor key

This device features 80-bit unique identification number, which is programmed in factory and loaded to SIM register after power-on reset.

2.1.10 Power management

These devices include on-chip LDO regulators and an on-chip DCDC converter to condition the main power supply voltage and allow for flexibility in power configurations. Three operating modes are supported: Bypass, LDO only, and DCDC (buck mode).

The SPM provides Stop (STOP), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), and Very Low Leakage Stop (VLLS) configurations in Arm’s Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

The Nested Vectored Interrupt Controller (NVIC), the Asynchronous Wake-up Interrupt Controller (AWIC), and the Low Leakage Wake-Up Controller (LLWU) are used to wake up the MCU from low power states. The NVIC is used to wake up the MCU core from WAIT and VLPW modes. The AWIC is used to wake up the MCU core from STOP and VLPS modes. The LLWU is used to wake up the MCU core from LLS and VLLS modes.

For additional information regarding operational modes, power management, the NVIC, AWIC, or the LLWU, please refer to the Reference Manual.

The following table shows module operations in different low power modes:

Table 7. Module operation in low power modes

Modules	VLPR	VLPW	STOP	VLPS	LLS	VLLS2/3	VLLS0/1
Core modules							
NVIC	FF	FF	SR	SR	SR	OFF	OFF
System modules							
MSMC	FF	FF	FF	FF	SR/FF[1]	OFF/FF[2]	OFF/FF[2]
LLWUx	FF	FF	FF	FF	FF	FF	FF
Core regulator (1.2 V)	Optional[3]	Optional[3]	Optional[3]	Optional[3]	Optional[3]	Optional[3]	Optional[3]
AUXREG 1.8 V	Optional[3]	Optional[3]	Optional[3]	Optional[3]	Optional[3]	Optional[3]	Optional[3]
HVD/LVD	Optional[4]	Optional[4]	Optional[4]	Optional[4]	Optional[4]	Optional[4]	Optional[4]
POR (Brown-Out)	FF	FF	FF	FF	FF	FF	Optional[5]
DMA	FF	FF	Async	Async	SR	OFF	OFF
Watchdog	FF	FF	Optional on with available clock source	Optional on with available clock source	SR	OFF	OFF
Clocks							
1 kHz LPO	FF	FF	FF	FF	FF	FF	Optional[6]
SCG	8 MHz SIRC	8 MHz SIRC	static – SIRC, FIRC, LPFLL optional	static – SIRC optional	static	OFF	OFF
Core clock	FF	OFF	OFF	OFF	OFF	OFF	OFF
Plat clock	FF	FF	OFF	OFF	OFF	OFF	OFF
Bus clock	FF	FF	OFF	OFF	OFF	OFF	OFF
Slow clock	FF	FF	OFF	OFF	OFF	OFF	OFF
Memory							
Flash	1 MHz No program	LP	LP	LP	SR	The registers are retained	OFF
SRAM	LP	LP	SR	Optional[7]	Optional[7]	Optional[7]	OFF
LPLMEM (Cache)	FF	FF	SR	SR	Optional retention	Optional[7]	OFF
LPCAC (Cache)	FF	FF	SR	SR	Optional retention	Optional[7]	OFF
System Register File	FF	FF	FF	FF	FF	FF	FF
VBAT Register File	Optional[8]	Optional[8]	Optional[8]	Optional[8]	Optional[8]	Optional[8]	Optional[8]
Communication Interface							

Table continues on the next page...

Table 7. Module operation in low power modes (continued)

Modules	VLPR	VLPW	STOP	VLPS	LLS	VLLS2/3	VLLS0/1
USB	static	static	static	static	static	OFF	OFF
USB Reg	Optional	Optional	Optional	Optional	Optional	Optional	Optional
LPUARTx	1 Mbit/s	1 Mbit/s	Async	Async	static	OFF	OFF
LPSPIx	Master 2 Mbit/s Slave 1 Mbit/s	Master 2 Mbit/s Slave 1 Mbit/s	Static, slave mode receive	Static, slave mode receive	static	OFF	OFF
LPI2Cx	1 Mbit/s	1 Mbit/s	Async	Async	static	OFF	OFF
I2S	FF	FF	Async	Async	static	OFF	OFF
EMVSIM	FF	FF	Static, card detect wakeup	Static, card detect wakeup	static	OFF	OFF
Timer modules							
LPTPMx	FF	FF	Async	Async	static	OFF	OFF
LPIT	FF	FF	Async	Async	static	OFF	OFF
LPTMRx	FF	FF	Async	Async	Async	FF	FF
RTC	FF	FF	Async	Async	Async	Optional[8]	Optional[8]
TSTMR	FF	FF	static	static	static	OFF	OFF
Security modules							
CAU3	FF	FF	static	static	static	OFF	OFF
CRC	FF	FF	static	static	static	OFF	OFF
Digital Tamper	FF	FF	Async	Async	Async	Optional[8]	Optional[8]
TRNG	FF	FF	static	static	static	OFF	OFF
Analog							
LPADC	FF	FF	LPADC internal clock	LPADC internal clock	SR	OFF	OFF
LPCMP0	FF	FF	FF	FF or Low power Nano mode Compare	FF or Low power Nano mode Compare	FF	FF[9]
LPCMP1	FF	FF	FF	FF or Low power Nano mode Compare	FF or Low power Nano mode Compare	Optional[10]	Optional[10]
6-bit DAC	FF	FF	static	static	static	OFF	OFF
12-bit LPDAC	FF	FF	static	static	static	OFF	OFF
VREF	FF	FF	static	static	static	OFF	OFF
HMI							
GPIO	FF	FF	Static output, wake up input	Static output, wake up input	Static, pins latched	OFF, pins latched	OFF, pins latched
FlexIO	FF	FF	Async	Async	SR	OFF	OFF

1. SR for reset related control and FF for power model related control
2. OFF for reset related control and FF for power model related control
3. It depends on MCU arbitration and SPM LPSEL/BGEN bit.
4. It depends on MCU arbitration and SPM LVDEN/BGEN/ALLREFN bit
5. It depends on MCU arbitration and SPM POREN bit.
6. It depends on MCU arbitration and SPM LPOEN/ALLREFN bit.
7. It depends on the configurations, see the next table for details.
8. Requires the VBAT supply to be properly powered.
9. It depends on SPM_CORELPCNFG[ALLREFEN] =1.
10. It depends on SPM_CORESC[VDDIOOVRIDE] = 1, SPM_CORELPCNFG[ALLREFEN] =1, and VDDIO2.

The following tables list all power mode combinations and corresponding power behaviors.

Table 8. MCU power mode combinations

CM4F power mode[1]	CM0+ power mode[2]	Max CM4F core clock frequency	Max CM0+ core clock frequency	MCU power mode[3]
RUN	RUN	48MHz	48MHz	RUN
RUN	HSRUN	72MHz	72MHz	HSRUN
RUN	VLPR	48MHz	48MHz	RUN
RUN	VLPW	48MHz	OFF	RUN
RUN	VLPS	48MHz	OFF	RUN
RUN	STOP/PSTOP	48MHz	OFF	RUN
RUN	LLS	48MHz	OFF	RUN
RUN	VLLS	48MHz	OFF	RUN
HSRUN	RUN	72MHz	72MHz	HSRUN
HSRUN	HSRUN	72MHz	72MHz	HSRUN
HSRUN	VLPR	72MHz	72MHz	HSRUN
HSRUN	VLPW	72MHz	OFF	HSRUN
HSRUN	VLPS	72MHz	OFF	HSRUN
HSRUN	STOP/PSTOP	72MHz	OFF	HSRUN
HSRUN	LLS	72MHz	OFF	HSRUN
HSRUN	VLLS	72MHz	OFF	HSRUN
VLPR	RUN	48MHz	48MHz	RUN
VLPR	HSRUN	72MHz	72MHz	HSRUN
VLPR	VLPR	8MHz	8MHz	VLP
VLPR	VLPW	8MHz	OFF	VLP
VLPR	VLPS	8MHz	OFF	VLP
VLPR	STOP/PSTOP	48MHz	OFF	RUN
VLPR	LLS	8MHz	OFF	VLP
VLPR	VLLS	8MHz	OFF	VLP
VLPW	RUN	OFF	48MHz	RUN
VLPW	HSRUN	OFF	72MHz	HSRUN
VLPW	VLPR	OFF	8MHz	VLP

Table continues on the next page...

Table 8. MCU power mode combinations (continued)

CM4F power mode[1]	CM0+ power mode[2]	Max CM4F core clock frequency	Max CM0+ core clock frequency	MCU power mode[3]
VLPW	VLPW	OFF	OFF	VLP
VLPW	VLPS	OFF	OFF	VLP
VLPW	STOP/PSTOP	OFF	OFF	RUN
VLPW	LLS	OFF	OFF	VLP
VLPW	VLLS	OFF	OFF	VLP
VLPS	RUN	OFF	48MHz	RUN
VLPS	HSRUN	OFF	72MHz	HSRUN
VLPS	VLPR	OFF	8MHz	VLP
VLPS	VLPW	OFF	OFF	VLP
VLPS	VLPS	OFF	OFF	VLP
VLPS	STOP/PSTOP	OFF	OFF	RUN
VLPS	LLS	OFF	OFF	VLP
VLPS	VLLS	OFF	OFF	VLP
STOP/PSTOP	RUN	OFF	48MHz	RUN
STOP/PSTOP	HSRUN	OFF	72MHz	HSRUN
STOP/PSTOP	VLPR	OFF	8MHz	RUN
STOP/PSTOP	VLPW	OFF	OFF	RUN
STOP/PSTOP	VLPS	OFF	OFF	RUN
STOP/PSTOP	STOP/PSTOP	OFF	OFF	RUN
STOP/PSTOP	LLS	OFF	OFF	RUN
STOP/PSTOP	VLLS	OFF	OFF	RUN
LLS	RUN	OFF	48MHz	RUN
LLS	HSRUN	OFF	72MHz	HSRUN
LLS	VLPR	OFF	8MHz	VLP
LLS	VLPW	OFF	OFF	VLP
LLS	VLPS	OFF	OFF	VLP
LLS	STOP/PSTOP	OFF	OFF	RUN
LLS	LLS	OFF	OFF	LLS
LLS	VLLS	OFF	OFF	LLS
VLLS	RUN	OFF	48MHz	RUN
VLLS	HSRUN	OFF	72MHz	HSRUN
VLLS	VLPR	OFF	8MHz	VLP
VLLS	VLPW	OFF	OFF	VLP
VLLS	VLPS	OFF	OFF	VLP
VLLS	STOP/PSTOP	OFF	OFF	RUN
VLLS	LLS	OFF	OFF	LLS
VLLS	VLLS	OFF	OFF	VLLS

1. It is configured by SMC0_PMCTRL register of MSMC.
2. It is configured by SMC1_PMCTRL register of MSMC.
3. It can be read out from SMCx_PMCSTAT register of MSMC. Please note the PMSTAT[7:0] bits in both SMC0_PMCSTAT and SMC1_PMCSTAT registers refer to MCU power mode so their value are identical. The STOPSTAT[31:24] bits in SMCx_PMCSTAT register reflect separate CM4F or CM0+ clock status, so can be different.

Table 9. Note

FF	Full functionality. In VLPR and VLPW, the system frequency is limited, but if a module does not have a limitation in its functionality, it is still listed as FF.
Async	Fully functional with alternate clock source, provided the selected clock source remains enabled
SR	Module state is retained but not functional.
LP	Module operates in a lower power state.
Off	Module is powered off and in reset state upon wake-up

The following table provides the modules that can wake MCU from low power modes.

Modules	VLPW	STOP	VLPS	LLS	VLLS3	VLLS1	VLLS0
RTC	Y	Y	Y	Y[1]	Y[1]	Y[1]	Y[2]
LPTMRx	Y	Y	Y	Y[1]	Y[1]	Y[1]	Y[3]
LPTPMx	Y	Y	Y	N	N	N	N
LPITx	Y	Y	Y	N	N	N	N
LLWUx	Y	Y	Y	Y	Y	Y	Y
LPSPIx	Y	Y	Y	N	N	N	N
LPI2Cx	Y	Y	Y	N	N	N	N
FlexIO	Y	Y	Y	N	N	N	N
LPUARTx	Y	Y	Y	N	N	N	N
USB	Y	Y	N	N	N	N	N
ADC	Y	Y	Y	N	N	N	N
LPCMPx	Y	Y	Y	Y[1]	Y[1]	Y[1]	N
LVD/HVD	Y	Y	Y	Y	Y	Y	Y
GPIO(except NMI,RESET)	Y	Y	Y	Y[4]	Y[4]	Y[4]	Y[4]
NMI	Y	Y	Y	Y	Y	Y	Y
RESET	Y	Y	Y	Y	Y	Y	Y

1. Need to configure this module as wakeup source of LLWU
2. Need to set EXTAL32 as RTC clock source and configure this module as wakeup source for LLWU
3. LPTMRs use EXTAL32 or LPO in VLLS0.
4. Only that pins available to configure to wakeup source of LLWU

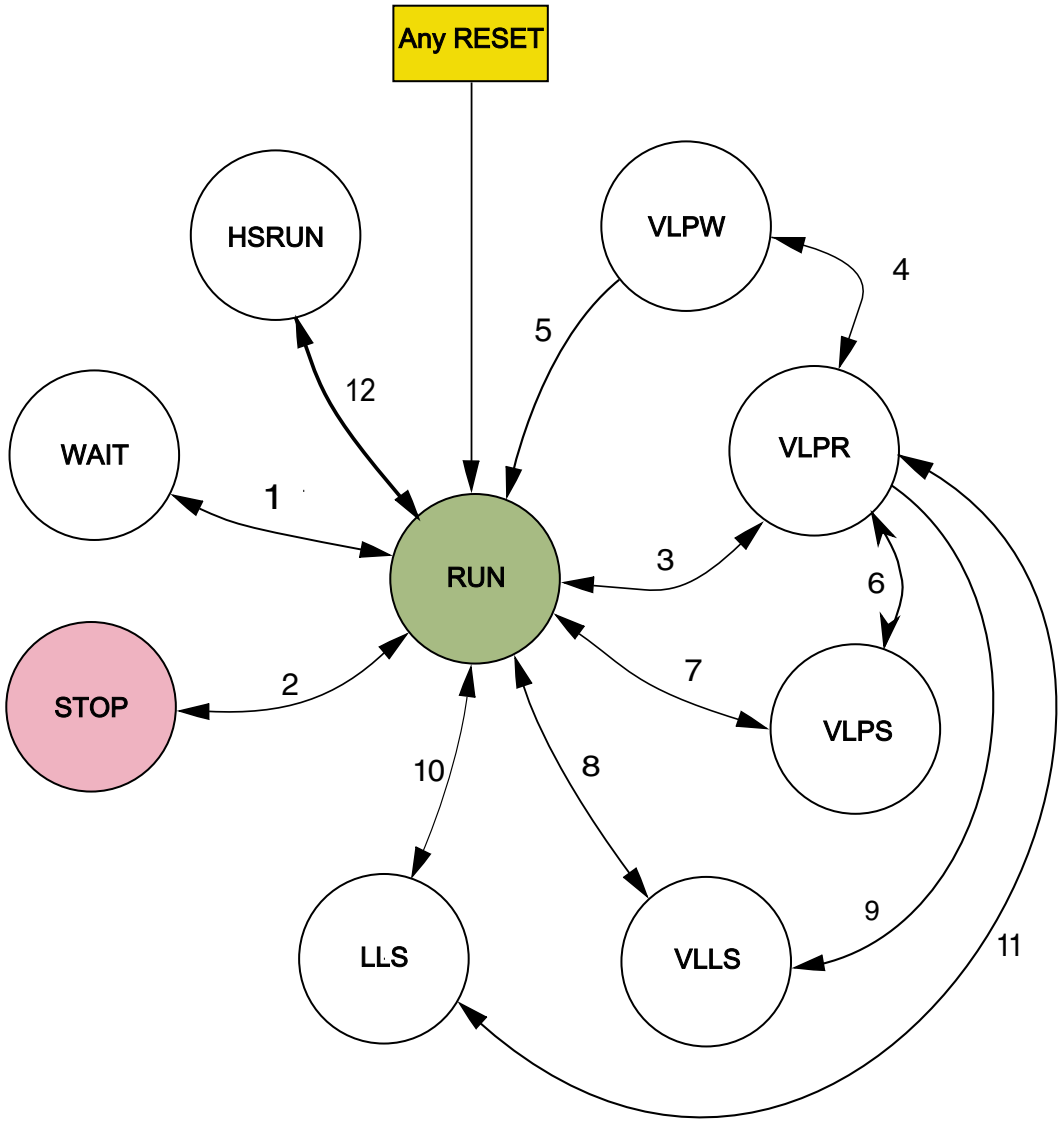


Figure 4. Power mode state transition diagram

2.1.11 LLWU

The LLWU module is used to wake MCU from low leakage power mode (LLS and VLLSx) and functional only on entry into a low-leakage power mode. After recovery from LLS, the LLWU is immediately disabled. After recovery from VLLSx, the LLWU continues to detect wake-up events until the user has acknowledged the wake-up event.

The following is internal peripheral and external pin inputs as wakeup sources for the Coretex-M4 core (CPU0).

Table 11. Wakeup Sources for LLWU0 inputs

LLWU0 pin	Module source or pin name
LLWU_P0	PTA1
LLWU_P1	PTA2
LLWU_P2	PTA22
LLWU_P3	PTA30
LLWU_P4	PTB1
LLWU_P5	PTB2
LLWU_P6	PTB4
LLWU_P7	PTB6
LLWU_P8	PTB7
LLWU_P9	PTB8
LLWU_P10	PTB16
LLWU_P11	PTB20
LLWU_P12	PTB22
LLWU_P13	PTB25
LLWU_P14	PTB28
LLWU_P15	PTC7
LLWU_P16	PTC9
LLWU_P17	PTC11
LLWU_P18	PTC12
LLWU_P19	PTD8
LLWU_P20	PTD10
LLWU_P21	PTE1[1]
LLWU_P22	PTE3[1]
LLWU_P23	PTE8[1]
LLWU_P24	PTE9[1]
LLWU_P25	PTE10[1]
LLWU_P26	PTE12[1]
LLWU_P27	Reserved[2]
LLWU_P28	Reserved[3]
LLWU_P29	USB0 VREGIN
LLWU_P30	USB0_DP[4]
LLWU_P31	USB0_DM[4]
LLWU_M0IF	LPTMR0, LPTMR1, LPTMR2 (sharing M0IF)[5]
LLWU_M1IF	LPCMP0[6]
LLWU_M2IF	LPCMP1[7]
LLWU_M3IF	Reserved[8]
LLWU_M4IF	Reserved[9]
LLWU_M5IF	Tamper Detect[10]

Table continues on the next page...

Table 11. Wakeup Sources for LLWU0 inputs (continued)

LLWU0 pin	Module source or pin name
LLWU_M6IF	RTC Alarm[10]
LLWU_M7IF	RTC Seconds[10]
LLWU_M0DR	LPTMR0 Asynchronous DMA
LLWU_M1DR	LPTMR1 Asynchronous DMA
LLWU_M2DR	LPTMR2 Asynchronous DMA
LLWU_M3DR	Reserved[11]
LLWU_M4DR	LPTMR0 Trigger
LLWU_M5DR	LPTMR1 Trigger
LLWU_M6DR	LPTMR2 Trigger
LLWU_M7DR	Reserved[12]

1. Set SPM_CORESC[VDDIOOVRIDE] for all PTE pins to wakeup from VLLS0/1
2. The corresponding LLWU0_PE[23: 22], LLWU0_PF[27], LLWU0_PDC2[27], and LLWU0_PMC[27] are reserved.
3. The corresponding LLWU0_PE[25: 24], LLWU0_PF[28], LLWU0_PDC2[28], and LLWU0_PMC[28] are reserved.
4. Set SPM_CORESC[USBOVRIDE] to wakeup from VLLS0 or VLLS1.
5. Requires the peripheral and the peripheral interrupt to be enabled. The LLWU's WUME bit enables the internal module flag as a wakeup input. After wakeup, the flags are cleared based on the peripheral clearing mechanism.
6. Set SPM_CORELPCNFG[ALLREFEN] to wakeup from VLLS0/1.
7. Set SPM_CORESC[VDDIOOVRIDE] and SPM_CORELPCNFG[ALLREFEN] to wakeup from VLLS0/1.
8. The corresponding LLWU0_ME[3] is reserved.
9. The corresponding LLWU0_ME[4] is reserved.
10. Set SPM_CORESC[VDDIOOVRIDE] to wakeup from VLLS0 or VLLS1.
11. The corresponding LLWU0_DE[3] is reserved.
12. The corresponding LLWU0_DE[7] is reserved.

The following is internal peripheral and external pin inputs as wakeup sources for the Coretex-M0+ core (CPU1).

Table 12. Wakeup Sources for LLWU1 inputs

LLWU1 pin	Module source or pin name
LLWU_P0	PTA1
LLWU_P1	PTA2
LLWU_P2	PTA22
LLWU_P3	PTA30
LLWU_P4	PTB1
LLWU_P5	PTB2
LLWU_P6	PTB4
LLWU_P7	PTB6
LLWU_P8	PTB7
LLWU_P9	PTB8
LLWU_P10	PTB16
LLWU_P11	PTB20

Table continues on the next page...

Table 12. Wakeup Sources for LLWU1 inputs (continued)

LLWU1 pin	Module source or pin name
LLWU_P12	PTB22
LLWU_P13	PTB25
LLWU_P14	PTB28
LLWU_P15	PTC7
LLWU_P16	PTC9
LLWU_P17	PTC11
LLWU_P18	PTC12
LLWU_P19	PTD8
LLWU_P20	PTD10
LLWU_P21	PTE1
LLWU_P22	PTE3
LLWU_P23	PTE8
LLWU_P24	PTE9
LLWU_P25	PTE10
LLWU_P26	PTE12
LLWU_P27	Reserved[1]
LLWU_P28	Reserved[2]
LLWU_P29	USB0 VREGIN
LLWU_P30	USB0_DP[-1]
LLWU_P31	USB0_DM[-1]
LLWU_M0IF	LPTMR0, LPTMR1, LPTMR2 (sharing M0IF)[3]
LLWU_M1IF	LPCMP0
LLWU_M2IF	LPCMP1
LLWU_M3IF	RESERVED[4]
LLWU_M4IF	Reserved[5]
LLWU_M5IF	Tamper Detect[-1]
LLWU_M6IF	RTC Alarm[-1]
LLWU_M7IF	RTC Seconds[-1]
LLWU_M0DR	LPTMR0 Asynchronous DMA
LLWU_M1DR	LPTMR1 Asynchronous DMA
LLWU_M2DR	LPTMR2 Asynchronous DMA
LLWU_M3DR	Reserved[6]
LLWU_M4DR	LPTMR0 Trigger
LLWU_M5DR	LPTMR1 Trigger
LLWU_M6DR	LPTMR2 Trigger
LLWU_M7DR	Reserved[7]

1. The corresponding LLWU1_PE[23:22], LLWU1_PF[27], LLWU1_PDC2[27], and LLWU1_PMC[27] are reserved.
2. The corresponding LLWU1_PE[25:24], LLWU1_PF[28], LLWU1_PDC2[28], and LLWU1_PMC[28] are reserved.

3. Requires the peripheral and the peripheral interrupt to be enabled. The LLWU's WUME bit enables the internal module flag as a wakeup input. After wakeup, the flags are cleared based on the peripheral clearing mechanism.
4. The corresponding LLWU1_ME[3] is reserved.
5. The corresponding LLWU1_ME[4] is reserved.
6. The corresponding LLWU1_DE[3] is reserved.
7. The corresponding LLWU1_DE[7] is reserved.

2.1.12 Debug controller

This device supports standard Arm 2-pin SWD and JTAG debug port. It provides register and memory accessibility from the external debugger interface, basic run/halt control plus 4 breakpoints and 2 watchpoints.

It also supports trace function with the Micro Trace Buffer (MTB), which provides a simple execution trace capability for the Cortex-M0+ processor.

2.1.13 INTMUX

The Interrupt Multiplexer (INTMUX) routes the interrupt sources to the interrupt outputs. It provides interrupt status registers to monitor interrupt pending status and vector numbers and implements the ability to logical AND or OR enabled interrupts on a given channel.

The INTMUX has the following features:

- Supports 4 multiplex channels
- Each channel receives 32 interrupt sources and has one interrupt output
- Each interrupt source can be enabled or disabled
- Each channel supports logic AND or logic OR of all enabled interrupt sources

2.1.14 FlexBus

The FlexBus multifunction external bus interface controller is a hardware module.

The FlexBus has the following features:

- 6 independent, user-programmable chip-select signals ($\overline{\text{FB_CS}}$5 – $\overline{\text{FB_CS}}$0)
- 8-bit, 16-bit, and 32-bit transfers
- Programmable burst and burst-inhibited transfers selectable for each chip-select and transfer direction
- Programmable address-setup time with reference to the assertion of a chip-select

- Programmable address-hold time with reference to the deassertion of a chip-select and transfer direction
- Extended address latch enable option to assist with glueless connections to synchronous and asynchronous memory devices

2.1.15 Watch dog

The Watchdog Timer (WDOG) keeps a watch on the system functioning and resets it in case of its failure.

The WDOG has the following features:

- Clock source input independent from CPU/bus clock. Choice from LPO, SIRC, external system clock or bus clock.
- Unlock sequence for allowing updates to write-once WDOG control/configuration bits.
- All WDOG control/configuration bits are writable once only within 128 bus clock cycles of being unlocked.
- Programmable time-out period specified in terms of number of WDOG clock cycles.
- Ability to test WDOG timer and reset with a flag indicating watchdog test.
- Windowed refresh option.
- Robust refresh mechanism.
- Count of WDOG resets as they occur.
- Configurable interrupt on time-out to provide debug breadcrumbs. This is followed by a reset after 128 bus clock cycles.

2.1.16 EWM

The External Watchdog Monitor (EWM) is a redundant watchdog system which is used to monitor external circuits, as well as the MCU software flow. This provides a back-up mechanism to the internal watchdog that resets the MCU's CPU and peripherals.

The EWM has the following features:

- Independent LPO_CLK clock source
- Programmable time-out period specified in terms of number of EWM LPO_CLK clock cycles.
- Windowed refresh option

    - Provides robust check that program flow is faster than expected.
    - Programmable window.
    - Refresh outside window leads to assertion of EWM_OUT_b.
- Robust refresh mechanism
    - Write values of 0xB4 and 0x2C to EWM Refresh Register within 15 peripheral bus clock cycles.
- One output port, EWM_OUT_b, when asserted is used to reset or place the external circuit into safe mode.
- One Input port, EWM_in, allows an external circuit to control the assertion of the EWM_OUT_b signal.

2.1.17 XRDC

The Extended Resource Domain Controller (XRDC) provides an integrated, scalable architectural framework for access control, system memory protection and peripheral isolation.

The XRDC has the following features:

- Assignment of chip resources to processing "domains"
    - Processor cores, non-core bus masters, slave memories and slave peripherals
    - Each processing domain is assigned a unique domain identifier (domainID, DID)
    - DomainID is a new attribute associated with every system bus transaction
    - Used in conjunction with user/privileged, secure/nonsecure attributes
- Access rights to slave targets defined in region descriptor registers for memories and access control registers for peripherals
- Supports sharing of memory and peripherals with optional inclusion of hardware semaphores to dynamically determine access rights
- Built upon a 4-level hierarchical access control model
    - PrivSecure > PrivNonsecure > UserSecure > UserNonsecure

    - Encoded into a 3-bit per-domain access control policy (ACP) used throughout the XRDC
    - Certain processors do not support the PrivNonsecure state. For these cores, the model simplifies to a 3-state definition: PrivSecure > UserSecure > UserNonsecure
- Programming model and hardware implementation is distributed across multiple submodules
    - Supports a broad, highly-configurable architecture definition
    - Memory region descriptors support a format leveraged from earlier System Memory Protection Units (SMPU)

2.1.18 MU

The Messaging Unit module enables two processors within the SoC to communicate and coordinate by passing messages (e.g. data, status and control) through the MU interface. The MU also provides the ability for one processor to signal the other processor using interrupts.

The MU has the following features:

- Messaging control by interrupts or by polling
- Symmetrical processor interfaces with each side supporting the following:
    - Three general-purpose flags reflected to the other side
    - Four general-purpose interrupt requests reflected to the other side
    - Four receive registers with maskable interrupt
    - Four transmit registers with maskable interrupt
- The Processor B can take the Processor A out of low-power modes by asserting one of the interrupts to the Processor A and vice versa

2.1.19 SEMA42

The SEMA42 is a memory-mapped module that provides robust hardware support needed in multi-core systems for implementing semaphores and provides a simple mechanism to achieve "lock and unlock" operations via a single write access. The hardware semaphore module provides hardware-enforced gates as well as other useful system functions related to the gating mechanisms.

The SEMA42 has the following features:

- Supports 16 hardware-enforced gates in a multi-processor configuration, where up to 15 processors can be supported; cp*X* is meant to represent core processor *X*
  - Gates appear as an 16-entry byte-size array with read and write accesses.
    - Processors lock gates by writing "processor_number+1" to the appropriate gate and must read back the gate value to verify the lock operation was successful.
    - Once locked, the gate is unlocked by a write of zeroes from the locking processor.
    - The number of implemented gates is specified by a hardware configuration define.
  - Each hardware gate appears as a 16-state, 4-bit state machine.
    - 16-state implementation

      if gate = 0x0, then state = unlocked
      if gate = 0x1, then state = locked by processor (master) 0
      if gate = 0x2, then state = locked by processor (master) 1
      …
      if gate = 0xF, then state = locked by processor (master) 14
    - Uses the logical bus master number as a reference attribute plus the specified data patterns to validate all write operations.
    - Once locked, the gate can (and must) be unlocked by a write of zeroes from the locking processor.
  - Secure reset mechanisms are supported to clear the contents of individual gates, as well as a clear_all capability.
- Memory-mapped IPS slave peripheral platform module
  - Interface to the IPS bus for programming-model accesses

2.1.20 TRGMUX

The trigger multiplexer (TRGMUX) module allows software to configure the trigger inputs for various peripherals.

The TRGMUX module allows software to select the trigger source for peripherals. Each peripheral has its own dedicated TRGMUX register.

2.2 Peripheral features

The following sections describe the features of each peripherals of the chip.

2.2.1 MSMC

The Multi-System Mode Controller (MSMC) is responsible for sequencing the MCU into and out of all stop and run power modes.

Specifically, it monitors events to trigger transitions between power modes while controlling the power, clocks, and memories of the MCU to achieve the power consumption and functionality of that mode. Additionally, the MSMC will arbitrate between multiple cores in the MCU to provide each with the most optimal power mode without negatively impacting the functionality of other cores.

2.2.2 CRC

This device contains one cyclic redundancy check (CRC) module which can generate 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial and other parameters required to implement a 16-bit or 32-bit CRC standard.

The 16/32-bit code is calculated for 32 bits of data at a time.

The CRC module has the following features:

- Hardware CRC generator circuit using a 16-bit or 32-bit programmable shift register
- Programmable initial seed value and polynomial
- Option to transpose input data or output data (the CRC result) bitwise or bytewise. This option is required for certain CRC standards. A bytewise transpose operation is not possible when accessing the CRC data register via 8-bit accesses. In this case, the user's software must perform the bytewise transpose function.
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

2.2.3 LPDAC

The 12-bit low power digital-to-analog converter (LPDAC) is a low-power, general-purpose DAC. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator or ADC.

LPDAC module has the following features:

- On-chip programmable reference generator output. The voltage output range is from 1⁄4096 V_{in} to V_{in}, and the step is 1⁄4096 V_{in}, where V_{in} is the input reference voltage.
- V_{in} can be selected from two reference sources.
- 16-word depth FIFO supported with configurable watermark.
- Multiple operation modes.
  - Buffer mode
  - FIFO mode
  - Swing back mode
- Software trigger and hardware trigger supported.
- Selectable performance levels: low power mode and high power mode.
- Interrupt and DMA support.

2.2.4 eDMA and DMAMUX

The eDMA controller module enables fast transfers of data, which provides an efficient way to move blocks of data with minimal processor interaction. The eDMA1 controller in this device implements eight channels which can be routed from up to 32 DMA request sources through DMAMUX1 module for CM0+ core. The eDMA0 module implements 16 channels which can be routed from up to 64 DMA request sources through DMAMUX0 module for CM4 core. Some of the peripheral request sources have asynchronous eDMA capability which can be used to wake MCU from Stop mode. The peripherals which have such capability include FlexIO, LPUART0, LPUART1, LPUART2, LPUART3, LPSPI0, LPSPI1, LPSPI2, LPSPI3, LPI2C0, LPI2C1, LPI2C2, LPI2C3, LPCMP0, LPCMP1, TPM0, TPM1, TPM2, TPM3,

LPTMR0, LPTMR1, LPTMR2, LLWU0, LLWU1, I2S, PORTA-PORTE, ADC0, and LPDAC0. The DMA0 channel 0 to 3 can be periodically triggered by LPIT0 while DMA1 channel 0 to 3 by LPIT1 via DMA MUX.

eDMA module has the following features:

- All data movement via dual-address transfers: read from source, write to destination
  - Programmable source and destination addresses and transfer size
  - Support for enhanced addressing modes
- 16-channel implementation that performs complex data transfers with minimal intervention from a host processor
  - Internal data buffer, used as temporary storage to support 16- and 32-byte transfers
  - Connections to the crossbar switch for bus mastering the data movement
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
  - 32-byte TCD stored in local memory for each channel
  - An inner data transfer loop defined by a minor byte transfer count
  - An outer data transfer loop defined by a major iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests, one per channel
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via programmable interrupt requests
  - One interrupt per channel, which can be asserted at completion of major iteration count
  - Programmable error terminations per channel and logically summed together to form one error interrupt to the interrupt controller

- Programmable support for scatter/gather DMA processing
- Support for complex data structures

DMAMUX module has the following features:

- Up to 64 peripheral slots can be routed to 16 channels for DMAMUX0 and up to 32 peripheral slots can be routed to 8 channels for DMAMUX1.
- 16 independently selectable DMA channel routers for DMAMUX0 and 8 for DMAMUX1.
- Each channel router can be assigned to one of the possible peripheral DMA slots.
- On every memory map configuration change for a any channel, this module signals to the DMA Controller to reset the internal state machine for that channel and it can accept a new request based on the new configuration.

2.2.5 EMV SIM

The EMV SIM (Euro/Mastercard/Visa Serial Interface Module) is designed to facilitate communication to Smart Cards compatible to the EMV ver4.3 standard (Book 1) and Smart Cards compatible with ISO/IEC 7816-3 Standard.

EMV-SIM module has the following features:

- Supports Smart Cards based on the EMV Standard v4.3 and ISO 7816-3 standard
- Independent clock for SIM logic (transmitter + receiver) and independent clock for register read-write interface
- 16 byte deep FIFO for transmitter and receiver
- Automatic NACK generation on parity error and receiver FIFO overflow error
- Support for both Inverse and Direct conventions
- Re-transmission of byte upon Smart Card NACK request with programmable threshold of re-transmissions
- Auto detection of Initial Character in receiver and setting of data format (inverse or direct)
- NACK detection in receiver
- Independent timers to measure character wait time, block wait time and block guard time
- Two general purpose counters available for use by software application with programmable clock selection for the counters
- DMA support available to transfer data to/from FIFOs. Programmable option available to select interrupt or DMA feature

- Programmable Prescaler to generate the desired frequency for Card Clock and Baud Rate Divisor to generate the internal ETU clocks for transmitter and receiver for any F/D ratio
- Deep sleep wake-up via Smart Card presence detect interrupt
- Manual control of all Smart Card interface signals
- Automatic power down of port logic on Smart Card presence detect
- Support for 8-bit LRC and 16-bit CRC generation for bytes sent out from transmitter and checking incoming message checksum for receiver

2.2.6 FlexIO

The FlexIO is a highly configurable module providing a wide range of protocols including, but not limited to LPUART, I2C, SPI, I2S, Camera IF, LCD RGB, PWM/ Waveform generation. The module supports programmable baud rates independent of bus clock frequency, with automatic start/stop bit generation. It also supports to work in VLPR, VLPW, Stop, and VLPS modes when clock source remains enabled.

The FlexIO module has the following features:

- Array of 32-bit shift registers with transmit, receive and data match modes
- Double buffered shifter operation for continuous data transfer
- Shifter concatenation to support large transfer sizes
- Automatic start/stop bit generation
- 1, 2, 4, 8, 16 or 32 multi-bit shift widths for parallel interface support
- Interrupt, DMA or polled transmit/receive operation
- Programmable baud rates independent of bus clock frequency, with support for asynchronous operation during stop modes
- Highly flexible 16-bit timers with support for a variety of internal or external trigger, reset, enable and disable conditions
- Programmable logic mode for integrating external digital logic functions on-chip or combining pin/shifter/timer functions to generate complex outputs
- Programmable state machine for offloading basic system control functions from CPU with support for up to 8 states, 8 outputs and 3 selectable inputs per state

2.2.7 LPADC

This device contains one low power ADC module. This LPADC module supports hardware triggers from TRGMUX. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

LPADC module has the following features:

- Linear successive approximation algorithm
  - single-ended operation with 12-bit resolution
- Channel support for up to 64 analog input channels for conversion of external pins and from internal sources
  - Measurement of on-chip analog sources such as DAC, temperature sensor or bandgap
- Configurable analog input sample time
- Configurable speed options to accommodate operation in low power modes of the device.
- Trigger detect with up to 4 trigger sources with priority level configuration. Software or hardware trigger option for each.
- 15 command buffers allow independent options selection and channel sequence scanning.
- Automatic compare for less-than, greater-than, within range, or out-of-range with "store on true" and "repeat until true" options
- 16-entry conversion result data FIFO with configurable watermark and overflow detection
- Interrupt, DMA or polled operation

2.2.8 LPCMP

The device contains two low power comparator modules which provide circuits for comparing two analog input voltages. Each comprises a comparator (CMP), a DAC and an analog mux (ANMUX).

The CMP circuit operates across the full range of the supply voltage. The DAC is a 64-tap resistor ladder network that provides a selectable voltage reference for applications requiring a voltage reference. The Analog MUX (ANMUX) provides a circuit for selecting an analog input signal from eight channels.

The LPCMP has the following features:

- Two 8-to-1 channel MUXes to select input signal from eight channels
- Multiple operation modes to produce a wide range of outputs such as:
  - Sampled

    - Windowed, which is ideal for certain PWM zero-crossing-detection applications
    - Digitally Filtered
- Selectable performance levels: nano mode, normal mode, high speed mode
- Programmable hysteresis control
- Selectable inversion on comparator output
- External hysteresis can be used at the same time that the output filter is used for internal functions
- Interrupt and DMA support
- Includes a 6-bit resolution DAC
- Selectable supply reference source for DAC
- Configurable low power mode or high speed mode for DAC

2.2.9 LPI2C

This device contains four LPI2C modules, which supports an efficient interface to an I2C bus as a master and/or a slave. The LPI2C can continue operating in stop modes provided an appropriate clock is available and is designed for low CPU overhead with DMA offloading of FIFO register accesses. The LPI2C implements logic support for standard-mode, fast-mode, fast-mode plus and ultra-fast modes of operation. The LPI2C module also complies with the System Management Bus (SMBus) Specification, version 2.

The LPI2C modules have the following features:

- Standard, Fast, Fast+ and Ultra Fast modes are supported
- High speed mode (HS) in slave mode
- High speed mode (HS) in master mode, if SCL pin implements current source pull-up (device-specific)
- Multi-master support, including synchronization and arbitration. Multi-master means any number of master nodes can be present. Additionally, master and slave roles may be changed between messages (after a STOP is sent).
- Clock stretching: Sometimes multiple I2C nodes may be driving the lines at the same time. If any I2C node is driving a line low, then that line will be low. I2C nodes that are starting to transmit a logical one (by letting the line float high) can

detect that the line is low, and thereby know that another I2C node is active at the same time.
    - When node detection is used on the SCL line, it is called *clock stretching*, and clock stretching is used as a I2C flow control mechanism for multiple laves.
    - When node detection is used on the SDA line, it is called *arbitration*, and arbitration ensures that there is only one I2C node transmitter at a time.
- General call, 7-bit and 10-bit addressing
- Software reset, START byte and Device ID (also require software support)

The LPI2C master supports:

- Command/transmit FIFO of 4words.
- Receive FIFO of 4words.
- Command FIFO will wait for idle I2C bus before initiating transfer
- Command FIFO can initiate (repeated) START and STOP conditions and one or more master-receiver transfers
- STOP condition can be generated from command FIFO, or generated automatically when the transmit FIFO is empty
- Host request input to control the start time of an I2C bus transfer
- Flexible receive data match can generate interrupt on data match and/or discard unwanted data
- Flag and optional interrupt to signal Repeated START condition, STOP condition, loss of arbitration, unexpected NACK, and command word errors
- Supports configurable bus idle timeout and pin-stuck-low timeout

The LPI2C slave supports:

- Separate I2C slave registers to minimize software overhead because of master/slave switching
- Support for 7-bit or 10-bit addressing, address range, SMBus alert and general call address
- Transmit data register that supports interrupt or DMA requests
- Receive data register that supports interrupt or DMA requests
- Software-controllable ACK or NACK, with optional clock stretching on ACK/NACK bit
- Configurable clock stretching, to avoid transmit FIFO underrun and receive FIFO overrun errors
- Flag and optional interrupt at end of packet, STOP condition, or bit error detection

2.2.10 LPIT

This device contains two LPIT modules which are multi-channel timer modules generating independent pre-trigger and trigger outputs. These timer channels can operate individually or can be chained together. The LPIT can operate in low power modes if configured to do so. The pre-trigger and trigger outputs can be used to trigger other modules on the device.

Each timer channel can be configured to run independently and made to work in either compare or capture modes.

The timer channels operate on an asynchronous clock, which is independent from the register read/write access clock. Clock synchronization between the clock domains ensures normal operations.

2.2.11 LPSPI

This device contains four low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus as a master and/or a slave. The LPSPI can continue operating in stop modes provided an appropriate clock is available and is designed for low CPU overhead with DMA offloading of FIFO register accesses.

The LPSPI supports:

- Word size = 32 bits
- Configurable clock polarity and clock phase
- Master operation supporting up to 4 peripheral chip select
- Slave operation
- Command/transmit FIFO of 4 words
- Receive FIFO of 4 words
- Flexible timing parameters in master mode, including SCK frequency and delays between PCS and SCK edges
- Support for full duplex transfers supporting 1-bit transmit and receive on each clock edge
- Support for half duplex transfers supporting 1-bit transmit or receive on each clock edge
- Support for half duplex transfers supporting 2-bit or 4-bit transmit or receive on each clock edge (master only)
- Host request input can be used to control the start time of an SPI bus transfer (master only)
- Receive data match logic supporting wakeup on data match

2.2.12 LPTMR

This device contains three low-power timer (LPTMR) which can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 32-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter
  - Rising-edge or falling-edge

2.2.13 LPUART

This product contains four Low-Power UART modules, their clock sources are selectable from LPFLL, SIRC, FIRC and SOSC, and can work in Stop and VLPS modes. They also support 4x to 32x data oversampling rate to meet different applications.

The LPUART module has the following features:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4x to 32x
- Transmit and receive baud rate can operate asynchronous to the bus clock:
  - Baud rate can be configured independently of the bus clock frequency
  - Supports operation in Stop modes
- Interrupt, DMA or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin

    - Break detect supporting LIN
    - Receive data match
- Hardware parity generation and checking
- Programmable 7-bit, 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods:
    - Idle line wakeup
    - Address mark wakeup
    - Receive data match
- Automatic address matching to reduce ISR overhead:
    - Address mark matching
    - Idle line address matching
    - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse width
- Independent FIFO structure for transmit and receive
    - Separate configurable watermark for receive and transmit requests
    - Option for receiver to assert request after a configurable number of idle characters if receive FIFO is not empty

2.2.14 RTC

The RTC is an always powered-on block that remains active in all low power modes. The time counter within the RTC is clocked by a 32.768 kHz clock sourced from an external crystal using the oscillator or clock directly from EXTAL32 pin.

RTC is reset on power-on reset, and a software reset bit in RTC can also initialize all RTC registers. During chip power-down, RTC is powered from the backup power supply (VBAT), electrically isolated from the rest of the chip, continues to increment the time counter (if enabled) and retain the state of the RTC registers. The RTC registers are not accessible.

The RTC module has the following features:

- Independent power supply, POR, and 32.768 kHz crystal oscillator
- 32-bit seconds counter with roll-over protection and 32-bit alarm
- 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
- Option to increment prescaler using a 1 kHz LPO (prescaler increments by 32 every clock edge)
- Register write protection
  - Lock register requires VBAT POR or software reset to enable write access
  - Access control registers require system reset to enable read and/or write access
- Configurable 1, 2, 4, 8, 16, 32, 64 or 128 Hz square wave output with optional interrupt
- 64-bit monotonic counter with roll-over protection
- Up to 4 tamper input pins with optional interrupt and seconds timestamp when interrupt asserts

2.2.15 I2S

This device contains one Inter-IC Sound (I2S) module which provides a synchronous audio interface (SAI) that supports fullduplex serial interfaces with frame synchronization such as I2S, AC97, TDM, and codec/DSP interfaces.

I2S module has the following features:

- Transmitter with independent bit clock and frame sync supporting 2 data lines
- Receiver with independent bit clock and frame sync supporting 2 data lines
- Each data line can support a maximum Frame size of 32 words
- Word size of between 8-bits and 32-bits
- Word size configured separately for first word and remaining words in frame
- Asynchronous 8 × 32-bit FIFO for each transmit and receive data line
- Supports graceful restart after FIFO error
- Supports automatic restart after FIFO error without software intervention
- Supports packing of 8-bit and 16-bit data into each 32-bit FIFO word
- Supports combining multiple data line FIFOs into single data line FIFO

2.2.16 uSDHC

The Ultra Secured Digital Host Controller (uSDHC) provides the interface between the host system and the SD/SDIO/MMC cards.

The uSDHC module has the following features:

- Conforms to the SD Host Controller Standard Specification version 2.0
- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41
- Compatible with the SD Memory Card Specification version 2.0 and supports the Extended Capacity SD Memory Card
- Compatible with the SDIO Card Specification version 2.0
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Card bus clock frequency up to 48 MHz
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes
- Supports single block/multi-block read and write
- Supports block sizes of 1 ~ 4096 bytes
- Supports the write protection switch for write operations
- Supports both synchronous and asynchronous abort
- Supports pause during the data transfer at block gap
- Supports SDIO Read Wait and Suspend Resume operations
- Supports Auto CMD12 for multi-block transfer
- Host can initiate non-data transfer command while data transfer is in progress
- Allows cards to interrupt the host in 1-bit and 4-bit SDIO modes, also supports interrupt period
- Embodies a fully configurable 128x32-bit FIFO for read/write data
- Supports internal DMA capabilities
- Support voltage selection by configuring vendor specific register bit
- Supports Advanced DMA to perform linked memory access

2.2.17 TPM

This device contains four low power TPM modules (TPM) which support input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. TPM0 and TPM2 have six channels while TPM1 and TPM3 have two channels.

The TPM modules have the following features:

- TPM clock mode is selectable

    - Can increment on every edge of the asynchronous counter clock
    - Can increment on rising edge of an external clock input synchronized to the asynchronous counter clock
- Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128
- TPM includes a 16-bit counter
    - It can be a free-running counter or modulo counter
    - The counting can be up or up-down
- Includes 6 channels that can be configured for input capture, output compare, edge-aligned PWM mode, or center-aligned PWM mode
    - In input capture mode the capture can occur on rising edges, falling edges or both edges
    - In output compare mode the output signal can be set, cleared, pulsed, or toggled on match
    - All channels can be configured for edge-aligned PWM mode or center-aligned PWM mode
- Support the generation of an interrupt and/or DMA request per channel
- Support the generation of an interrupt and/or DMA request when the counter overflows
- Support selectable trigger input to optionally reset or cause the counter to start incrementing.
    - The counter can also optionally stop incrementing on counter overflow
- Support the generation of hardware triggers when the counter overflows and per channel

2.2.18 TRNG

The Standalone True Random Number Generator (SA-TRNG) is a hardware accelerator module that generates a 128-bit entropy as needed by an entropy-consuming module or by other post-processing functions.

2.2.19 USB

This device contains one USB module which implements a USB2.0 full-speed compliant peripheral and interfaces to the on-chip USBFS transceiver. It implements keep-alive feature to avoid re-enumerating when exiting from low power modes and enables FIRC48M to allow crystal-less USB operation.

The USBFS has the following features:

- USB 1.1 and 2.0 compatible FS device
- 16 bidirectional endpoints
- DMA or FIFO data stream interfaces
- Low-power consumption
- IRC48M with clock-recovery is supported to eliminate the 48 MHz crystal. It is used for USB device-only implementation.
- Keep-alive feature is supported to power down system bus and CPU. USB can respond to IN with NAK and wake up for SETUP/OUT.

2.2.20 VREF

The VREF can be used in applications to provide a reference voltage to external devices, or used internally in the device as a reference to analog peripherals (such as the ADC, LPDAC, or LPCMP). The Voltage Reference (VREF) can supply an accurate voltage output that can be trimmed in 0.5 mV steps (for 1.2 V output) or 1.5 mV steps (for 2.1 V output). The voltage reference has 3 operating modes that provide different levels of supply rejection and power consumption.

The VREF supports the following features:

A 100 nF capacitor must always be connected between VERF output (VREFO) pin and VSSA if the VREF is used. This capacitor must be as close to VREFO pin as possible.

2.2.21 TSTMR

The Time Stamp Timer (TSTMR) is a 56-bit clock cycle counter, reset by system reset.

The TSTMR has the following features:

- Free-running Time Stamp Timer

2.2.22 CAU3

The Version 3 Cryptographic Acceleration Unit (CAU3) is a bus mastering IP module that provides hardware acceleration of a variety of cryptographic symmetric key and secure hash algorithms including DES, 3DES, AES-{128,192,256}, SHA-{1,256} as well as acceleration of basic public key cryptography including Elliptical Curve Cryptography (ECC). The execution of these algorithms is controlled by optimized firmware developed by NXP that executes on the CAU3 module.

The CAU3 has the following features:

- Symmetric key functions: DES, 3DES, AES-{128,192,256}
- Secure hash functions: SHA-1, SHA-256
- Supoort secure hash acceleration
- AES-CBC, AES-CCM
- RSA and ECC acceleration
- Programmable task completion signaling: interrupt, event completion, DMA request
- Significantly improved performance and power efficiency
- Common, portable CAU3 library written in C
- Arm embedded TLS library reference design

2.3 Memory map

This device contains various memories and memory-mapped peripherals which are located in a 4 GB memory space. The following figure shows the system memory and peripheral locations

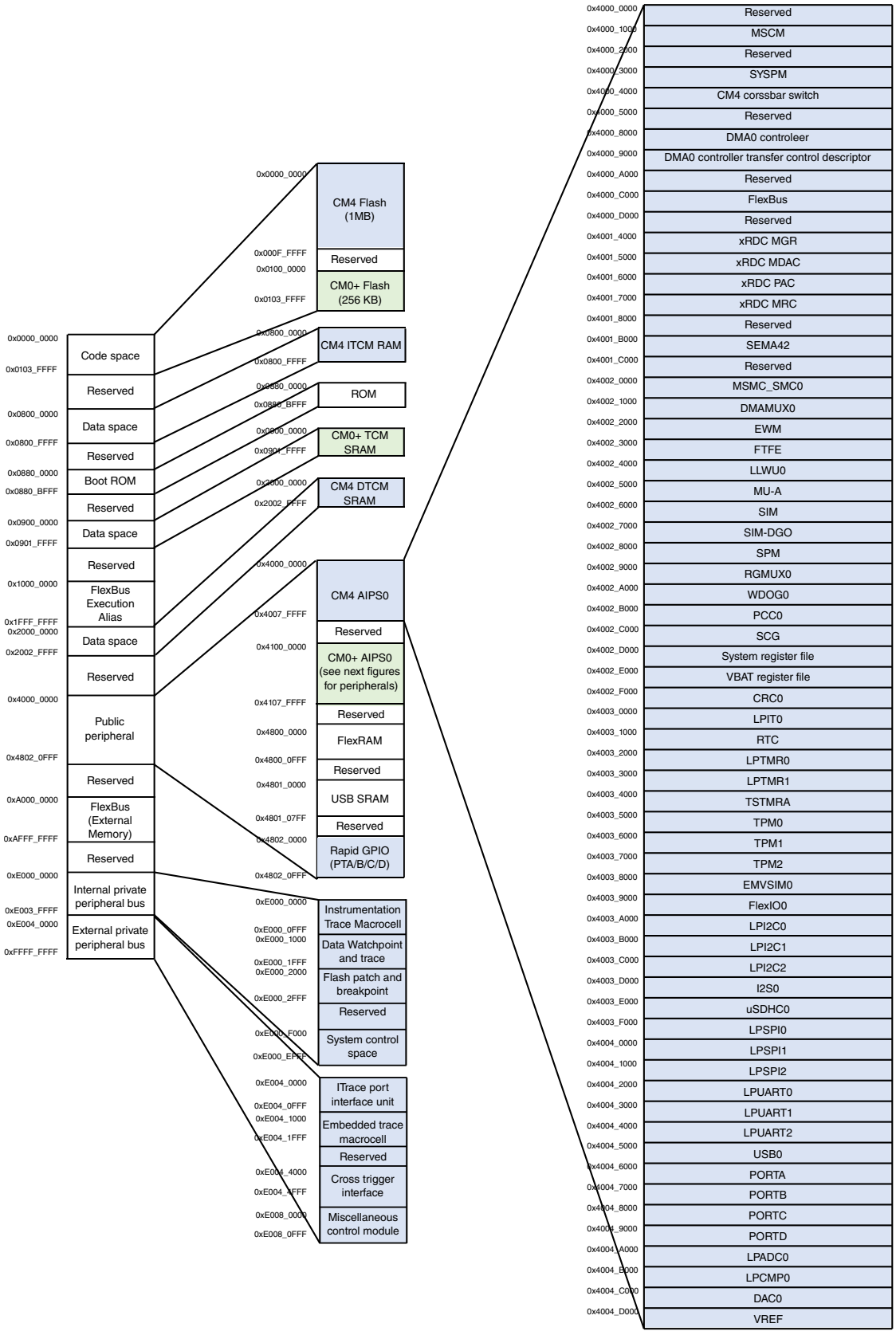


Figure 5. Memory map (CM4)

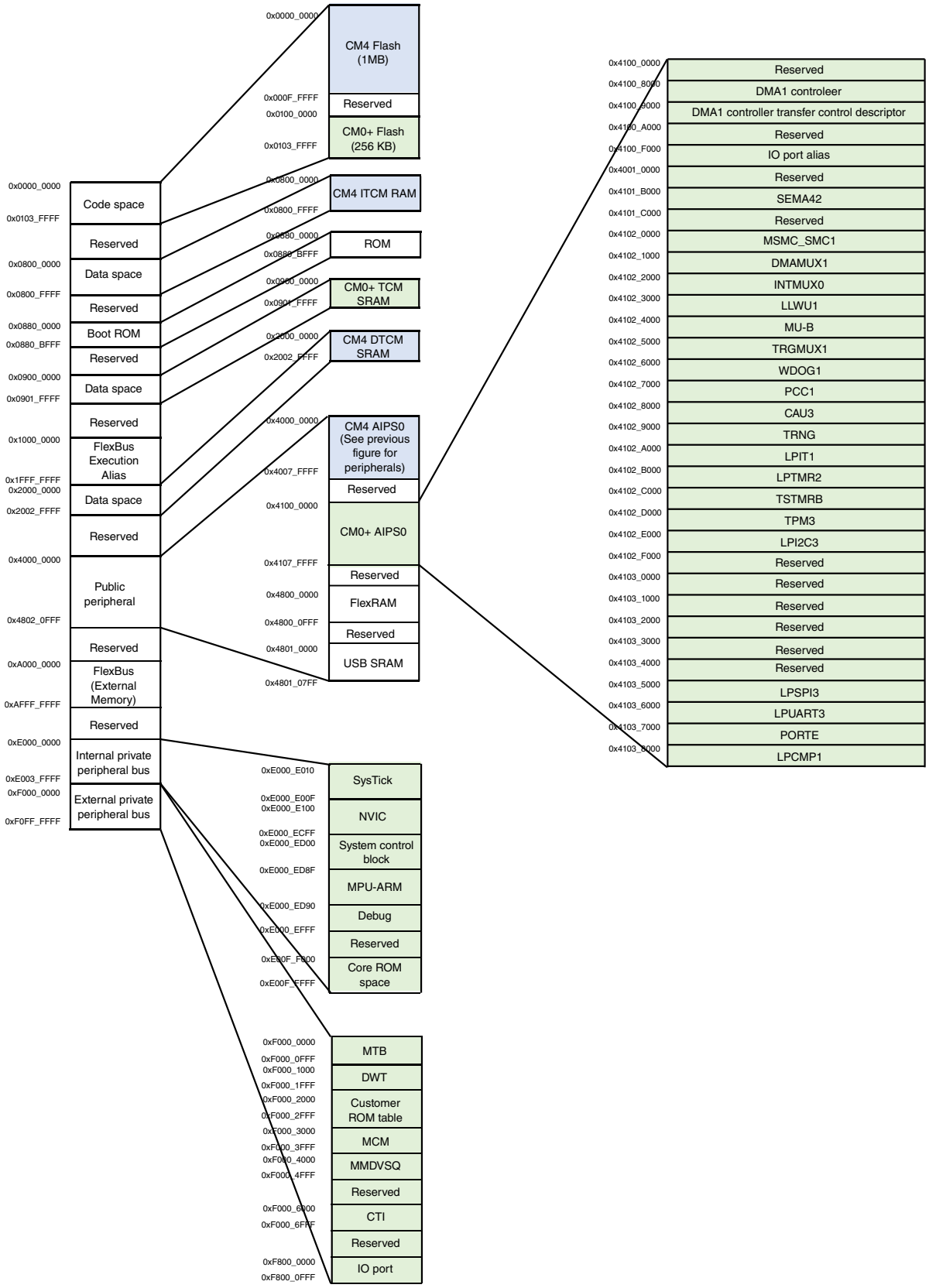


Figure 6. Memory map (CM0+)

3 Pinouts

3.1 K32 subfamily pinout

Table 13. K32 Pinout

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
C1	PTB3	LPADC0_SE0	LPADC0_SE0	PTB3	LPSPI0_PCS3	LPUART1_TX	I2S0_TX_FS	FB_AD10	TPM0_CH1	—
C2	PTB4/LLWU_P6	LPADC0_SE1	LPADC0_SE1	PTB4/LLWU_P6	LPSPI0_SCK	LPUART1_CTS	I2S0_TX_BCLK	FB_AD9	TPM0_CH2	—
D2	PTB5	DISABLED	—	PTB5	LPSPI0_SOUT	LPUART1_RTS	I2S0_MCLK	FB_AD8	TPM0_CH3	—
E1	PTB6/LLWU_P7	DISABLED	—	PTB6/LLWU_P7	LPSPI0_PCS2	LPI2C1_SDA	I2S0_RX_BCLK	FB_AD7	TPM0_CH4	—
E2	PTB7/LLWU_P8	LPADC0_SE2	LPADC0_SE2	PTB7/LLWU_P8	LPSPI0_SIN	LPI2C1_SDAS	I2S0_RX_FS	FB_AD6	TPM0_CH5	—
F5	PTB8/LLWU_P9	DISABLED	—	PTB8/LLWU_P9	LPSPI0_PCS0	LPI2C1_SCLS	I2S0_RXD0	FB_AD5	—	LPTMR0_ALT1
F4	PTB9	LPADC0_SE3	LPADC0_SE3	PTB9/SPM_LPREQ	LPSPI0_PCS1	LPI2C1_SCL	I2S0_RXD1	FB_RW_b	—	FXIO0_D0
D5	VSS	VSS	VSS	—	—	—	—	—	—	—
C9	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
G6	PTB11	DISABLED	—	PTB11	LPUART2_RX	LPI2C1_SDAS	LPI2C0_SDA	FB_AD27	—	FXIO0_D1
G4	PTB12	DISABLED	—	PTB12	LPUART2_TX	LPI2C1_SCLS	LPI2C0_SCL	FB_AD26	TPM3_CLKIN	FXIO0_D2
G3	PTB13	DISABLED	—	PTB13	LPUART2_CTS	LPI2C1_SDA	LPI2C0_SDAS	FB_AD25	TPM3_CH0	FXIO0_D3
G2	PTB14	DISABLED	—	PTB14	LPUART2_RTS	LPI2C1_SCL	LPI2C0_SCLS	FB_AD24	TPM3_CH1	FXIO0_D4
G1	PTB15	DISABLED	—	PTB15	—	LPI2C1_HREQ	LPI2C3_SCL	FB_CS5_b/FB_TSIZ1/FB_BE23_16_b	TPM0_CLKIN	FXIO0_D5

Table continues on the next page...

Table 13. K32 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
H5	PTB16/ LLWU_P10	DISABLED	—	PTB16/ LLWU_P10	—	LPUART3_CTS	LPI2C3_SDA	FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_b	—	FXIO0_D6
K5	PTB17	DISABLED	—	PTB17	—	LPUART3_RTS	LPI2C3_SCLS	FB_TBST_b/ FB_CS2_b/ FB_BE15_8_b	—	FXIO0_D7
H2	PTB18	DISABLED	—	PTB18	LPSPI1_PCS1	LPUART2_RX	LPI2C3_SDAS	FB_CS3_b/ FB_BE7_0_b	FB_TA_b	FXIO0_D8
K4	PTB19	DISABLED	—	PTB19	LPSPI1_PCS3	LPUART2_TX	—	FB_ALE/ FB_CS1_b/ FB_TS_b	TPM1_CLKIN	FXIO0_D9
J1	PTB20/ LLWU_P11	DISABLED	—	PTB20/ LLWU_P11	LPSPI1_SCK	LPUART2_CTS	—	FB_CS0_b	TPM1_CH0	FXIO0_D10
J2	PTB21	DISABLED	—	PTB21	LPSPI1_SOUT	LPUART2_RTS	LPI2C2_HREQ	FB_AD4	TPM1_CH1	FXIO0_D11
L1	PTB22/ LLWU_P12	DISABLED	—	PTB22/ LLWU_P12	LPSPI1_PCS2	LPUART0_CTS	LPI2C2_SDA	FB_AD3	TPM2_CLKIN	FXIO0_D12
J4	VSS	VSS	VSS	—	—	—	—	—	—	—
J3	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
L2	PTB24	DISABLED	—	PTB24	LPSPI1_SIN	LPUART0_RTS	LPI2C2_SCL	FB_AD2	EWM_IN	FXIO0_D13
L6	PTB25/ LLWU_P13	DISABLED	—	PTB25/ LLWU_P13	LPSPI1_PCS0	LPUART0_RX	LPI2C2_SDAS	FB_AD1	EWM_OUT_b	FXIO0_D14
L4	PTB26	DISABLED	—	PTB26	USB0_SOF_OUT	LPUART0_TX	LPI2C2_SCLS	FB_AD0	LPCMP0_OUT	—
M4	PTB28/ LLWU_P14	DISABLED	—	PTB28/ LLWU_P14	—	LPUART3_RX	I2S0_TXD0	FB_A16	—	FXIO0_D15
L3	PTB29	DISABLED	—	PTB29	—	LPUART3_TX	I2S0_TX_FS	FB_A17	—	FXIO0_D16
M5	PTB30	DISABLED	—	PTB30	—	—	I2S0_TX_BCLK	FB_A18	—	—
M7	PTB31	DISABLED	—	PTB31	—	—	I2S0_RXD0	FB_A19	—	—

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Table 13. K32 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
N1	PTC0	DISABLED	—	PTC0	—	—	I2S0_RX_FS	FB_A20	—	—
M2	PTC1	DISABLED	—	PTC1	—	—	I2S0_RX_BCLK	FB_A21	—	—
N3	VSS	VSS	VSS	—	—	—	—	—	—	—
J10	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
N2	PTC7/ LLWU_P15	LPCMP0_IN0	LPCMP0_IN0	PTC7/ LLWU_P15	LPSPI0_PCS3	LPUART0_RX	LPI2C1_HREQ	—	TPM0_CH0	LPTMR1_ALT1
P3	PTC8	LPCMP0_IN1	LPCMP0_IN1	PTC8	LPSPI0_SCK	LPUART0_TX	LPI2C0_HREQ	—	TPM0_CH1	—
R1	PTC9/ LLWU_P16	LPADC0_SE4/ LPCMP0_IN2	LPADC0_SE4/ LPCMP0_IN2	PTC9/ LLWU_P16	LPSPI0_SOUT	LPUART0_CTS	LPI2C0_SDA	—	TPM0_CH2	LPTMR0_ALT2
R2	PTC10	LPADC0_SE5	LPADC0_SE5	PTC10	LPSPI0_PCS2	LPUART0_RTS	LPI2C0_SCL	—	TPM0_CH3	—
T1	PTC11/ LLWU_P17	LPADC0_SE6	LPADC0_SE6	PTC11/ LLWU_P17	LPSPI0_SIN	LPI2C1_SDA	LPI2C0_SDAS	—	TPM0_CH4	EWM_IN
R3	PTC12/ LLWU_P18	LPADC0_SE7	LPADC0_SE7	PTC12/ LLWU_P18	LPSPI0_PCS0	LPI2C1_SCL	LPI2C0_SCLS	—	TPM0_CH5	EWM_OUT_b
U1	VDD_DCDC	VDD_DCDC	VDD_DCDC	—	—	—	—	—	—	—
U2	LP	LP	LP	—	—	—	—	—	—	—
U3	GND	GND	GND	—	—	—	—	—	—	—
T4	LN	LN	LN	—	—	—	—	—	—	—
T3	VOUT_AUX	VOUT_AUX	VOUT_AUX	—	—	—	—	—	—	—
T5	VOUT_CORE	VOUT_CORE	VOUT_CORE	—	—	—	—	—	—	—
R9	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
P9	VSS	VSS	VSS	—	—	—	—	—	—	—
N15	VDD_CORE	VDD_CORE	VDD_CORE	—	—	—	—	—	—	—
P6	PTC27	DISABLED	—	PTC27	—	—	—	—	TPM0_CH4	—
U5	PTC28	DISABLED	—	PTC28	—	LPSPI0_PCS1	—	—	TPM0_CH3	FXIO0_D17
N6	PTC29	DISABLED	—	PTC29	LPUART1_RX	LPSPI0_PCS3	—	—	TPM0_CH2	FXIO0_D18

Table continues on the next page...

Table 13. K32 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
R7	PTC30	DISABLED	—	PTC30	LPUART1_TX	LPSPI0_SCK	—	—	TPM0_CH1	FXIO0_D19
R5	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
R13	VSS	VSS	VSS	—	—	—	—	—	—	—
T7	PTD0	DISABLED	—	PTD0	LPUART1_CTS	LPSPI0_SOUT	—	—	TPM0_CH0	FXIO0_D20
P7	PTD1	DISABLED	—	PTD1	LPUART1_RTS	LPSPI0_PCS2	—	—	EWM_IN	FXIO0_D21
U7	PTD2	DISABLED	—	PTD2	SDHC0_D7	LPSPI0_SIN	—	—	EWM_OUT_b	FXIO0_D22
T8	PTD3	DISABLED	—	PTD3	SDHC0_D6	LPSPI0_PCS0	EMVSIM0_CLK	—	TPM2_CLKIN	FXIO0_D23
N8	PTD4	DISABLED	—	PTD4	SDHC0_D5	LPSPI2_PCS1	EMVSIM0_RST	—	—	FXIO0_D24
N10	PTD5	LPADC0_SE8	LPADC0_SE8	PTD5	SDHC0_D4	LPSPI2_PCS3	EMVSIM0_VCCEN	—	—	FXIO0_D25
U9	PTD6	LPADC0_SE9	LPADC0_SE9	PTD6	SDHC0_D1	LPSPI2_SCK	EMVSIM0_IO	TRACE_D3	TPM2_CH5	FXIO0_D26
P10	PTD7	LPADC0_SE10	LPADC0_SE10	PTD7	SDHC0_D0	LPSPI2_SOUT	EMVSIM0_PD	TRACE_D2	TPM2_CH4	FXIO0_D27
T9	PTD8/LLWU_P19	LPADC0_SE11	LPADC0_SE11	PTD8/LLWU_P19	SDHC0_DCLK	LPSPI2_PCS2	LPI2C1_SDAS	TRACE_D1	TPM2_CH3	FXIO0_D28
U11	PTD9	LPADC0_SE12	LPADC0_SE12	PTD9	SDHC0_CMD	LPSPI2_SIN	LPI2C1_SCLS	TRACE_D0	TPM2_CH2	FXIO0_D29
P11	PTD10/LLWU_P20	LPADC0_SE13	LPADC0_SE13	PTD10/LLWU_P20	SDHC0_D3	LPSPI2_PCS0	LPI2C1_SDA	TRACE_CLKOUT	TPM2_CH1	FXIO0_D30
R11	PTD11	LPADC0_SE14	LPADC0_SE14	PTD11	SDHC0_D2	USB0_SOF_OUT	LPI2C1_SCL	CLKOUT	TPM2_CH0	FXIO0_D31
P5	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
P13	VSS	VSS	VSS	—	—	—	—	—	—	—
N4	USB0_VSS	USB0_VSS	USB0_VSS	—	—	—	—	—	—	—
T11	USB0_DP	USB0_DP	USB0_DP	—	—	—	—	—	—	—
T12	USB0_DM	USB0_DM	USB0_DM	—	—	—	—	—	—	—
T13	VOUT33	VOUT33	VOUT33	—	—	—	—	—	—	—
U13	VREGIN	VREGIN	VREGIN	—	—	—	—	—	—	—
U15	VDDA	VDDA	VDDA	—	—	—	—	—	—	—
U16	VREFH	VREFH	VREFH	—	—	—	—	—	—	—

Table continues on the next page...

Table 13. K32 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
T15	VREF_OUT	VREF_OUT/ LPADC0_SE15/ LPCMP0_IN5/ LPCMP1_IN5	VREF_OUT/ LPADC0_SE15/ LPCMP0_IN5/ LPCMP1_IN5	—	—	—	—	—	—	—
U17	VREFL	VREFL	VREFL	—	—	—	—	—	—	—
T16	VSSA	VSSA	VSSA	—	—	—	—	—	—	—
T17	DAC0_OUT	DAC0_OUT/ LPADC0_SE16/ LPCMP0_IN3/ LPCMP1_IN3	DAC0_OUT/ LPADC0_SE16/ LPCMP0_IN3/ LPCMP1_IN3	—	—	—	—	—	—	—
R14	PTE0	LPCMP1_IN4	LPCMP1_IN4	PTE0	—	—	—	—	EWM_IN	—
R16	PTE1/ LLWU_P21	LPADC0_SE18	LPADC0_SE18	PTE1/ LLWU_P21	SDHC0_D1	LPI2C0_SDAS	LPSPI3_PCS1	—	EWM_OUT_b	LPTMR1_ALT2
P12	PTE2	LPADC0_SE19	LPADC0_SE19	PTE2	SDHC0_D0	LPI2C0_SCLS	LPSPI3_PCS3	—	LPCMP1_OUT	—
N12	PTE3/ LLWU_P22	LPADC0_SE20/ LPCMP1_IN0	LPADC0_SE20/ LPCMP1_IN0	PTE3/ LLWU_P22	SDHC0_D7	LPI2C0_SDA	LPSPI3_SCK	—	TPM0_CLKIN	LPTMR0_ALT3
M11	PTE4	LPADC0_SE21/ LPCMP1_IN1	LPADC0_SE21/ LPCMP1_IN1	PTE4	SDHC0_D6	LPI2C0_SCL	LPSPI3_SOUT	CLKOUT	TPM1_CLKIN	—
R17	PTE5	LPCMP1_IN2	LPCMP1_IN2	PTE5	SDHC0_DCLK	LPI2C0_HREQ	LPSPI3_PCS2	—	LPCMP1_OUT	—
J8	VDD_CORE	VDD_CORE	VDD_CORE	—	—	—	—	—	—	—
K10	VSS	VSS	VSS	—	—	—	—	—	—	—
D13	VDDIO2	VDDIO2	VDDIO2	—	—	—	—	—	—	—
P16	PTE8/ LLWU_P23	LPADC0_SE22	LPADC0_SE22	PTE8/ LLWU_P23	SDHC0_D5	LPUART3_RX	LPSPI3_SIN	—	TPM1_CH0	LPTMR2_ALT1
N16	PTE9/ LLWU_P24	LPADC0_SE23	LPADC0_SE23	PTE9/ LLWU_P24	SDHC0_CMD	LPUART3_TX	LPSPI3_PCS0	—	TPM1_CH1	FXIO0_D0

Table continues on the next page...

Table 13. K32 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
M13	PTE10/ LLWU_P25	DISABLED	—	PTE10/ LLWU_P25	SDHC0_D4	LPUART3_CTS	LPI2C3_SDA	—	TPM3_CH0	LPTMR2_ALT3
M14	PTE11	DISABLED	—	PTE11	SDHC0_D3	LPUART3_RTS	LPI2C3_SCL	—	TPM3_CH1	FXIO0_D1
L12	PTE12/ LLWU_P26	DISABLED	—	PTE12/ LLWU_P26	SDHC0_D2	—	LPI2C3_SDAS	—	TPM3_CLKIN	FXIO0_D2
N17	PTE13	DISABLED	—	PTE13	I2S0_TX_BCLK	—	LPI2C3_SCLS	—	TPM3_CH0	FXIO0_D3
L16	PTE14	DISABLED	—	PTE14	I2S0_TX_FS	—	LPI2C3_HREQ	—	TPM3_CH1	FXIO0_D4
L17	PTE15	DISABLED	—	PTE15	I2S0_TXD0	—	—	—	TPM3_CLKIN	FXIO0_D5
L14	PTE16	DISABLED	—	PTE16	I2S0_RX_BCLK	—	—	—	TPM2_CH0	FXIO0_D6
L15	PTE17	DISABLED	—	PTE17	I2S0_RX_FS	—	—	—	TPM2_CH1	FXIO0_D7
K13	PTE18	DISABLED	—	PTE18	I2S0_RXD0	—	—	—	TPM2_CH2	FXIO0_D8
K16	PTE19	DISABLED	—	PTE19	I2S0_MCLK	—	—	—	TPM2_CH3	FXIO0_D9
J17	PTE21	DISABLED	—	PTE21	I2S0_TXD1	USB0_SOF_OUT	—	—	TPM2_CH4	FXIO0_D10
J16	PTE22	DISABLED	—	PTE22	I2S0_RXD1	LPI2C3_HREQ	—	—	TPM2_CH5	FXIO0_D11
J14	VSS	VSS	VSS	—	—	—	—	—	—	—
J15	VDDIO2	VDDIO2	VDDIO2	—	—	—	—	—	—	—
H14	PTE27	DISABLED	—	PTE27	LPUART3_CTS	LPI2C3_SDAS	—	—	—	FXIO0_D28
G14	PTE28	DISABLED	—	PTE28	LPUART3_RTS	LPI2C3_SCLS	—	—	—	FXIO0_D29
G15	PTE29	DISABLED	—	PTE29	LPUART3_RX	LPI2C3_SDA	—	—	—	FXIO0_D30
G17	PTE30	DISABLED	—	PTE30	LPUART3_TX	LPI2C3_SCL	—	—	TPM2_CLKIN	FXIO0_D31
H13	TAMPER3/ RTC_CLKOUT	TAMPER3/ RTC_CLKOUT	TAMPER3/ RTC_CLKOUT	—	—	—	—	—	—	—
G12	TAMPER2/ RTC_CLKOUT	TAMPER2/ RTC_CLKOUT	TAMPER2/ RTC_CLKOUT	—	—	—	—	—	—	—

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Table 13. K32 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
F13	TAMPER1/ RTC_CLKOUT	TAMPER1/ RTC_CLKOUT	TAMPER1/ RTC_CLKOUT	—	—	—	—	—	—	—
F14	TAMPER0/ RTC_WAKEUP_b	TAMPER0/ RTC_WAKEUP_b	TAMPER0/ RTC_WAKEUP_b	—	—	—	—	—	—	—
G16	VBAT	VBAT	VBAT	—	—	—	—	—	—	—
E17	XTAL32	XTAL32	XTAL32	—	—	—	—	—	—	—
E16	EXTAL32	EXTAL32	EXTAL32	—	—	—	—	—	—	—
E15	VSS	VSS	VSS	—	—	—	—	—	—	—
C17	NC[1]	NC	NC	—	—	—	—	—	—	—
B17	NC[1]	NC	NC	—	—	—	—	—	—	—
A16	VSS	VSS	VSS	—	—	—	—	—	—	—
A15	NC[1]	NC	NC	—	—	—	—	—	—	—
B13	NC[1]	NC	NC	—	—	—	—	—	—	—
A11	NC[1]	NC	NC	—	—	—	—	—	—	—
B11	NC[1]	NC	NC	—	—	—	—	—	—	—
C11	NC[1]	NC	NC	—	—	—	—	—	—	—
D12	RESET_b	RESET_b	RESET_b	—	—	—	—	—	—	—
B10	PTA0	NMI_b	—	PTA0	—	—	—	—	—	NMI_b
E12	PTA1/ LLWU_P0	JTAG_TCLK/ SWD_CLK	—	PTA1/ LLWU_P0	LPUART0_CTS	LPI2C0_SDAS	LPUART1_CTS	—	—	JTAG_TCLK/ SWD_CLK
F11	PTA2/ LLWU_P1	JTAG_TDI	—	PTA2/ LLWU_P1	LPUART0_RX	LPI2C0_SDA	LPUART1_RX	—	—	JTAG_TDI
D11	PTA3	JTAG_TDO/ SWD_SWO	—	PTA3	LPUART0_TX	LPI2C0_SCL	LPUART1_TX	—	TPM0_CLKIN	JTAG_TDO/ SWD_SWO
B9	PTA4	JTAG_TMS/ SWD_DIO	—	PTA4	LPUART0_RTS	LPI2C0_SCLS	LPUART1_RTS	—	LPCMP0_OUT	JTAG_TMS/ SWD_DIO
H9	VDD_CORE	VDD_CORE	VDD_CORE	—	—	—	—	—	—	—
E14	VSS	VSS	VSS	—	—	—	—	—	—	—
K9	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—

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Table 13. K32 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
E10	PTA9	DISABLED	—	PTA9	LPI2C2_SDAS	LPSPI3_SCK	—	FB_A23	—	—
A9	PTA10	DISABLED	—	PTA10	LPI2C2_SCLS	LPSPI3_SOUT	—	FB_A22	—	—
E8	PTA14	DISABLED	—	PTA14	LPI2C2_SDA	—	—	FB_AD23	LPCMP0_OUT	—
A7	PTA15	DISABLED	—	PTA15	LPI2C2_SCL	—	—	FB_AD22	—	—
A17	VSS	VSS	VSS	—	—	—	—	—	—	—
E4	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
F7	PTA17	DISABLED	—	PTA17	LPI2C2_HREQ	LPSPI3_PCS1	EMVSIM0_CLK	FB_AD21	—	—
D8	PTA18	DISABLED	—	PTA18	LPSPI2_PCS1	LPSPI3_PCS3	EMVSIM0_RST	FB_AD20	—	—
D7	PTA19	DISABLED	—	PTA19	LPSPI2_PCS3	LPSPI3_SCK	EMVSIM0_VCCEN	FB_AD19	TPM2_CH5	—
C7	PTA20	DISABLED	—	PTA20	LPSPI2_SCK	LPSPI1_PCS1	EMVSIM0_IO	FB_AD18	TPM2_CH4	—
B7	PTA21	DISABLED	—	PTA21	LPSPI2_SOUT	—	EMVSIM0_PD	FB_AD17	TPM2_CH3	—
B6	PTA22/LLWU_P2	DISABLED	—	PTA22/LLWU_P2	LPSPI2_PCS2	—	LPI2C2_HREQ	FB_AD16	TPM2_CH2	—
E6	PTA23	DISABLED	—	PTA23	LPSPI2_SIN	LPSPI1_PCS3	LPI2C2_SDA	FB_AD15	TPM2_CH1	—
D6	PTA24	DISABLED	—	PTA24	LPSPI2_PCS0	LPSPI1_SCK	LPI2C2_SCL	FB_OE_b	TPM2_CH0	—
B5	PTA25	DISABLED	—	PTA25	LPUART1_RX	LPSPI3_SOUT	LPI2C2_SDAS	FB_AD31	—	—
A5	PTA26	DISABLED	—	PTA26	LPUART1_TX	LPSPI3_PCS2	LPI2C2_SCLS	FB_AD30	—	—
A3	PTA27	DISABLED	—	PTA27	LPUART1_CTS	LPSPI3_SIN	—	FB_AD29	—	—
A2	PTA28	DISABLED	—	PTA28	LPUART1_RTS	LPSPI3_PCS0	—	FB_AD28	—	—
A13	VSS	VSS	VSS	—	—	—	—	—	—	—
E3	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
A1	PTA30/LLWU_P3	DISABLED	—	PTA30/LLWU_P3	LPUART2_CTS	LPSPI1_SOUT	—	FB_AD14	TPM1_CH0	LPTMR2_ALT2
C4	PTA31	DISABLED	—	PTA31	LPUART2_RTS	LPSPI1_PCS2	—	FB_AD13	TPM1_CH1	—

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Table 13. K32 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
B3	PTB0	DISABLED	—	PTB0	LPUART2_TX	LPSPI1_SIN	USB0_SOF_OUT	CLKOUT	TPM1_CLKIN	—
C3	PTB1/ LLWU_P4	DISABLED	—	PTB1/ LLWU_P4	LPUART2_RX	LPSPI1_PCS0	I2S0_TXD1	FB_AD12	—	LPTMR1_ALT3
B1	PTB2/ LLWU_P5	DISABLED	—	PTB2/ LLWU_P5	LPSPI0_PCS1	LPUART1_RX	I2S0_TXD0	FB_AD11	TPM0_CH0	—
B14	VSS	VSS	VSS	—	—	—	—	—	—	—
B15	VSS	VSS	VSS	—	—	—	—	—	—	—
B16	VSS	VSS	VSS	—	—	—	—	—	—	—
C5	VSS	VSS	VSS	—	—	—	—	—	—	—
C13	VSS	VSS	VSS	—	—	—	—	—	—	—
C15	VSS	VSS	VSS	—	—	—	—	—	—	—
C16	VSS	VSS	VSS	—	—	—	—	—	—	—
D9	VSS	VSS	VSS	—	—	—	—	—	—	—
D15	VSS	VSS	VSS	—	—	—	—	—	—	—
F16	VSS	VSS	VSS	—	—	—	—	—	—	—
H8	VSS	VSS	VSS	—	—	—	—	—	—	—
H10	VSS	VSS	VSS	—	—	—	—	—	—	—
K8	VSS	VSS	VSS	—	—	—	—	—	—	—
N14	VDD_CORE	VDD_CORE	VDD_CORE	—	—	—	—	—	—	—
R15	VSSA	VSSA	VSSA	—	—	—	—	—	—	—
T2	VDD_DCDC	VDD_DCDC	VDD_DCDC	—	—	—	—	—	—	—
B2	PTA30/ LLWU_P3	DISABLED	—	PTA30/ LLWU_P3	LPUART2_CTS	LPSPI1_SOUT	—	FB_AD14	TPM1_CH0	LPTMR2_ALT2

1. The NC pins must be floating.

3.2 Pin properties

The following table lists the pin properties.

Table 14. Pin properties

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
C1	PTB3	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
C2	PTB4/ LLWU_ P6	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
D2	PTB5	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
E1	PTB6/ LLWU_ P7	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
E2	PTB7/ LLWU_ P8	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
F5	PTB8/ LLWU_ P9	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
F4	PTB9	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
D5	VSS	—	—	—	—	—	—	—	—	—	—	—
C9	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
G6	PTB11	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
G4	PTB12	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
G3	PTB13	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
G2	PTB14	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
G1	PTB15	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
H5	PTB16/ LLWU_ P10	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
K5	PTB17	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
H2	PTB18	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N

Table continues on the next page...

Table 14. Pin properties (continued)

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
K4	PTB19	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
J1	PTB20/ LLWU_ P11	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
J2	PTB21	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L1	PTB22/ LLWU_ P12	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
J4[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
J3	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
L2	PTB24	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L6	PTB25/ LLWU_ P13	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L4	PTB26	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
M4	PTB28/ LLWU_ P14	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L3	PTB29	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
M5	PTB30	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
M7	PTB31	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
N1	PTC0	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
M2	PTC1	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
N3[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
J10	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
N2	PTC7/ LLWU_ P15	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
P3	PTC8	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y

Table continues on the next page...

Table 14. Pin properties (continued)

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
R1	PTC9/ LLWU_ P16	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
R2	PTC10	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
T1	PTC11/ LLWU_ P17	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
R3	PTC12/ LLWU_ P18	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
U1	VDD_D CDC	—	—	—	—	—	—	—	—	—	—	—
U2	LP	—	—	—	—	—	—	—	—	—	—	—
U3	GND	—	—	—	—	—	—	—	—	—	—	—
T4	LN	—	—	—	—	—	—	—	—	—	—	—
T3	VOUT_ AUX	—	—	—	—	—	—	—	—	—	—	—
T5	VOUT_ CORE	—	—	—	—	—	—	—	—	—	—	—
R9	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
P9	VSS	—	—	—	—	—	—	—	—	—	—	—
N15	VDD_C ORE	—	—	—	—	—	—	—	—	—	—	—
—	PTC26	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
P6	PTC27	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
U5	PTC28	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
N6	PTC29	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
R7	PTC30	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
R5	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
R13	VSS	—	—	—	—	—	—	—	—	—	—	—

Table continues on the next page...

Table 14. Pin properties (continued)

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
T7	PTD0	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
P7	PTD1	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
U7	PTD2	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
T8	PTD3	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
N8	PTD4	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
N10	PTD5	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
U9	PTD6	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
P10	PTD7	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
T9	PTD8/ LLWU_ P19	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
U11	PTD9	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
P11	PTD10/ LLWU_ P20	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
R11	PTD11	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
P5	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
P13[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
N4	USB0_ VSS	—	—	—	—	—	—	—	—	—	—	—
T11	USB0_ DP	—	—	—	—	—	—	—	—	—	—	—
T12	USB0_ DM	—	—	—	—	—	—	—	—	—	—	—
T13	VOUT33	—	—	—	—	—	—	—	—	—	—	—
U13	VREGIN	—	—	—	—	—	—	—	—	—	—	—
U15	VDDA	—	—	—	—	—	—	—	—	—	—	—
U16	VREFH	—	—	—	—	—	—	—	—	—	—	—

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Table 14. Pin properties (continued)

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
T15	VREF_OUT	—	—	—	—	—	—	—	—	—	—	—
U17	VREFL	—	—	—	—	—	—	—	—	—	—	—
T16	VSSA	—	—	—	—	—	—	—	—	—	—	—
T17	DAC0_OUT	—	—	—	—	—	—	—	—	—	—	—
R14	PTE0	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
R16	PTE1/ LLWU_P21	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
P12	PTE2	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
N12	PTE3/ LLWU_P22	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
M11	PTE4	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
R17	PTE5	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
J8	VDD_CORE	—	—	—	—	—	—	—	—	—	—	—
K10[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
D13	VDDIO2	—	—	—	—	—	—	—	—	—	—	—
P16	PTE8/ LLWU_P23	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
N16	PTE9/ LLWU_P24	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
M13	PTE10/ LLWU_P25	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
M14	PTE11	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y

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Table 14. Pin properties (continued)

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
L12	PTE12/ LLWU_ P26	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
N17	PTE13	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L16	PTE14	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L17	PTE15	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L14	PTE16	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L15	PTE17	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
K13	PTE18	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
K16	PTE19	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
J17	PTE21	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
J16	PTE22	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
J14[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
J15	VDDIO2	—	—	—	—	—	—	—	—	—	—	—
H14	PTE27	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
G14	PTE28	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
G15	PTE29	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
G17	PTE30	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
H13	TAMPE R3	ND	Hi-Z	N	PU	FS	N	N	N	N	N	N
G12	TAMPE R2	ND	Hi-Z	N	PU	FS	N	N	N	N	N	N
F13	TAMPE R1/ RTC_C LKOUT	ND	Hi-Z	N	PU	FS	N	N	N	N	N	N

Table continues on the next page...

Table 14. Pin properties (continued)

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
F14	TAMPER0/ RTC_WAKEUP_b	ND	Hi-Z	N	PU	FS	N	N	N	N	N	N
G16	VBAT	—	—	—	—	—	—	—	—	—	—	—
E17	XTAL32	—	—	—	—	—	—	—	—	—	—	—
E16	EXTAL32	—	—	—	—	—	—	—	—	—	—	—
E15	VSS	—	—	—	—	—	—	—	—	—	—	—
C17	NC[2]	—	—	—	—	—	—	—	—	—	—	—
B17	NC[2]	—	—	—	—	—	—	—	—	—	—	—
A16	VSS	—	—	—	—	—	—	—	—	—	—	—
A15	NC[2]	—	—	—	—	—	—	—	—	—	—	—
B13	NC[2]	—	—	—	—	—	—	—	—	—	—	—
A11	NC[2]	—	—	—	—	—	—	—	—	—	—	—
B11	NC[2]	—	—	—	—	—	—	—	—	—	—	—
C11	NC[2]	—	—	—	—	—	—	—	—	—	—	—
D12	RESET_b	ND	H	N	PU	—	Y	—	—	—	—	—
B10	PTA0	ND	H	Y	PU	FS	N	N	Y	Y	N	N
E12	PTA1/ LLWU_P0	ND	L	Y	PD	FS	N	N	Y	Y	N	N
F11	PTA2/ LLWU_P1	ND	H	Y	PU	FS	N	N	Y	Y	N	N
D11	PTA3	ND	H	Y	PU	FS	N	N	Y	Y	N	N
B9	PTA4	ND	H	Y	PU	FS	N	N	Y	Y	N	N

Table continues on the next page...

Table 14. Pin properties (continued)

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
H9	VDD_CORE	—	—	—	—	—	—	—	—	—	—	—
E14	VSS	—	—	—	—	—	—	—	—	—	—	—
K9	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
E10	PTA9	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
A9	PTA10	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
E8	PTA14	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
A7	PTA15	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
A17[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
E4	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
F7	PTA17	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
D8	PTA18	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
D7	PTA19	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
C7	PTA20	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
B7	PTA21	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
B6	PTA22/ LLWU_P2	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
E6	PTA23	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
D6	PTA24	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
B5	PTA25	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
A5	PTA26	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
A3	PTA27	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
A2	PTA28	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
A13[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
E3	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
A1	PTA30/ LLWU_P3	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N

Table continues on the next page...

Table 14. Pin properties (continued)

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
C4	PTA31	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
B3	PTB0	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
C3	PTB1/ LLWU_ P4	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
B1	PTB2/ LLWU_ P5	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
B14	VSS	—	—	—	—	—	—	—	—	—	—	—
B15	VSS	—	—	—	—	—	—	—	—	—	—	—
B16	VSS	—	—	—	—	—	—	—	—	—	—	—
C5[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
C13[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
C15[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
C16[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
D9	VSS	—	—	—	—	—	—	—	—	—	—	—
D15	VSS	—	—	—	—	—	—	—	—	—	—	—
F16[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
H8[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
H10[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
K8	VSS	—	—	—	—	—	—	—	—	—	—	—
N14	VDD_C ORE	—	—	—	—	—	—	—	—	—	—	—
R15[1]	VSSA	—	—	—	—	—	—	—	—	—	—	—
T2	VDD_D CDC	—	—	—	—	—	—	—	—	—	—	—
B2	PTA30/ LLWU_ P3	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N

1. Optional, can be left as NC.

2. The NC pins must be floating.

Properties	Abbreviation	Descriptions
Driver strength	ND	Normal drive
	HD	High drive
Default status after POR	Hi-Z	High impendence
	H	High level
	L	Low level
Pullup/ pulldown Enable after POR	Y	Enabled
	N	Disabled
Pullup/ pulldown selection after POR	PU	Pullup
	PD	Pulldown
Slew rate after POR	FS	Fast slew rate
	SS	Slow slew rate
Passive Pin Filter after POR	N	Disabled
	Y	Enabled
Open drain	N	Disabled[1]
	Y	Enabled
Pin interrupt	Y	Yes
Fast capability	N	Not support fast capability
	Y	Support fast capability
Fast high drive	N	Not support fast high drive
	Y	Support fast high drive

1. When an LPI2C module is enabled and a pin is functional for LPI2C, this pin is (pseudo-) open drain enabled. When an LPUART module is enabled and a pin is functional for LPUART, this pin is (pseudo-) open drain configurable.

3.3 Module signal description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

3.3.1 Core modules

Table 15. JTAG Arm signal descriptions

Chip signal name	Module signal name	Description	I/O
JTAG_TMS	TMS	Test mode select	Input
JTAG_TCLK	TCK	Test clock	Input

Table continues on the next page...

Table 15. JTAG Arm signal descriptions (continued)

Chip signal name	Module signal name	Description	I/O
JTAG_TDI	TDI	Test data in	Input
JTAG_TDO	TDO	Test data out	Output

Table 16. SWD signal descriptions

Chip signal name	Module signal name	Description	I/O
SWD_DIO	SWD_DIO	Serial wire data input/output. The SWD_DIO pin is used by an external debug tool for communication and device control. This pin is pulled up internally.	Input / Output
SWD_CLK	SWD_CLK	Serial wire clock. This pin is the clock for debug logic when in the Serial Wire Debug mode. This pin is pulled down internally.	Input
SWD_SWO	SWD_SWO	Trace output over a single pin	Output

Table 17. TPIU signal descriptions

Chip signal name	Module signal name	Description	I/O
TRACE_CLKOUT	TRACECLK	Trace clock output from the Arm CoreSight debug block	O
TRACE_D[3:2]	TRACEDATA	Trace output data from the Arm CoreSight debug block used for 5-pin interface	O
TRACE_D[1:0]	TRACEDATA	Trace output data from the Arm CoreSight debug block used for both 5-pin and 3-pin interfaces	O

3.3.2 System modules

Table 18. System signal descriptions

Chip signal name	Module signal name	Description	I/O
NMI_b	—	Non-maskable interrupt **NOTE:** Driving the $\overline{\text{NMI}}$ signal low forces a non-maskable interrupt, if the $\overline{\text{NMI}}$ function is selected on the corresponding pin.	I
RESET_b	—	Reset bi-directional signal	I/O
VDD_CORE	—	MCU power	I
VDDIO1	—	I/O rings power	I
VDDIO2	—	I/O rings power	I
VSS	—	MCU ground	I

Table continues on the next page...

Table 18. System signal descriptions (continued)

Chip signal name	Module signal name	Description	I/O
VSSA	—	Analog ground	I

Table 19. EWM signal descriptions

Chip signal name	Module signal name	Description	I/O
EWM_IN	EWM_in	EWM input for safety status of external safety circuits. The polarity of EWM_in is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low.	I
EWM_OUT_b	$\overline{\text{EWM\_out}}$	EWM reset out signal	O

Table 20. LLWU0 signal descriptions

Chip signal name	Module signal name	Description	I/O
LLWU_Pn (n=[31:0]	LLWU_Pn (n=[31:0]	External Pin Wakeup inputs	I

3.3.3 Memories and memory interfaces

Table 21. FlexBus signal descriptions

Chip signal name	Module signal name	Description	I/O
FB_CLKOUT	FB_CLK	FlexBus Clock Output	O
FB_A[23:16]	FB_A[23:16]	This is the address and data bus	I/O
FB_AD[31:0]	FB_ADn	This is the address and data bus, FB_AD. The number of byte lanes carrying the data is determined by the port size associated with the matching chip-select. The full 32-bit address is driven on the first clock of a bus cycle (address phase). After the first clock, the data is driven on the bus (data phase). During the data phase, the address is driven on the pins not used for data. For example, in 16-bit mode, the lower address is driven on FB_AD15–FB_AD0, and in 8-bit mode, the lower address is driven on FB_AD23–FB_AD0.	I/O
FB_CSn_b (n=[5:0])	$\overline{\text{FB_CS}}$n (n=[5:0])	General Purpose Chip-Selects—Indicate which external memory or peripheral is selected. A particular chip-select is asserted when the transfer address is within the external memory's or peripheral's address space, as defined in CSAR[BA] and CSMR[BAM].	O

Table continues on the next page...

Table 21. FlexBus signal descriptions (continued)

Chip signal name	Module signal name	Description	I/O
FB_BE31_24_b FB_BE23_16_b FB_BE15_8_b FB_BE7_0_b	FB_BE_31_24, FB_BE_23_16, FB_BE_15_8, FB_BE_7_0	Byte Enables—Indicate that data is to be latched or driven onto a specific byte lane of the data bus. CSCR[BEM] determines if these signals are asserted on reads and writes or on writes only. For external SRAM or flash devices, the FB_BE outputs should be connected to individual byte strobe signals.	O
FB_OE_b	FB_OE	Output Enable—Sent to the external memory or peripheral to enable a read transfer. This signal is asserted during read accesses only when a chip-select matches the current address decode.	O
FB_RW_b	FB_RW	Read/Write—Indicates whether the current bus operation is a read operation (FB_R/W high) or a write operation (FB_R/W low).	O
FB_TS_b	FB_TS	Transfer Start—Indicates that the chip has begun a bus transaction and that the address and attributes are valid.	O
FB_ALE	FB_ALE	Address Latch Enable—Indicates when the address is being driven on the FB_A bus (inverse of FB_TS).	O
FB_TSIZn (n=[1:0])	FB_TSIZn (n=[1:0])	Transfer Size—Indicates (along with FB_TBST) the data transfer size of the current bus operation. The interface supports 8-, 16-, and 32-bit operand transfers and allows accesses to 8-, 16-, and 32-bit data ports.	O
FB_TA_b	FB_TA	Transfer Acknowledge—Indicates that the external data transfer is complete. When FB_TA is asserted during a read transfer, FlexBus latches the data and then terminates the transfer. When FB_TA is asserted during a write transfer, the transfer is terminated.	I
FB_TBST_b	FB_TBST	Transfer Burst—Indicates that a burst transfer is in progress as driven by the chip. A burst transfer can be 2 to 16 beats depending on FB_TSIZ1–FB_TSIZ0 and the port size.	O

3.3.4 Clock modules

Table 22. RTC OSC signal descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL32	EXTAL32	32.768 kHz oscillator input	I
XTAL32	XTAL32	32.768 kHz oscillator output	O

3.3.5 Communication interfaces

Table 23. EMVSIM signal descriptions

Chip signal name	Module signal name	Description	I/O
EMVSIM0_CLK	EMVSIM_SCLK	Card Clock. Clock to Smart Card.	O
EMVSIM0_RST	EMVSIM_SRST	Card Reset. Reset signal to Smart Card	O
EMVSIM0_VCCEN	EMVSIM_VCC_EN	Card Power Enable. This signal controls the power to Smart Card	O
EMVSIM0_IO	EMVSIM_IO	Card Data Line. Bi-directional data line.	I/O
EMVSIM0_PD	EMVSIM_PD	Card Presence Detect. Signal indicating presence or removal of card	I

Table 24. USB FS signal descriptions

Chip signal name	Module signal name	Description	I/O
USB0_DM	usb_dm	USB D- analog data signal on the USB bus.	I/O
USB0_DP	usb_dp	USB D+ analog data signal on the USB bus.	I/O
USB_SOF_OUT	—	USB start of frame signal. Can be used to make the USB start of frame available for external synchronization.	O
USB0_VSS	—	V_{SS} for USB0	—

Table 25. USB VREG signal descriptions

Chip signal name	Module signal name	Description	I/O
VOUT33	reg33_out	Regulator output voltage	O
VREGIN	vreg_in1	Unregulated power supply	I

Table 26. LPSPI0 signal descriptions

Chip signal name	Module signal name	Description	I/O
SPI0_SCK	SCK	Serial clock. Input in slave mode, output in master mode.	I/O
SPI0_PCS0	PCS[0]	Peripheral Chip Select. Input in slave mode, output in master mode.	I/O
SPI0_PCS1	PCS[1]	Peripheral Chip Select or Host Request. Host Request pin is selected when HREN=1 and HRSEL=0. Input in either slave mode or when used as Host Request, output in master mode.	I/O
SPI0_PCS2	PCS[2]	Peripheral Chip Select or data pin 2 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O

Table continues on the next page...

Table 26. LPSPI0 signal descriptions (continued)

Chip signal name	Module signal name	Description	I/O
SPI0_PCS3	PCS[3]	Peripheral Chip Select or data pin 3 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O
SPI0_SOUT	SOUT	Serial Data Output. Can be configured as serial data input signal. Used as data pin 0 in quad-data and dual-data transfers.	I/O
SPI0_SIN	SIN	Serial Data Input. Can be configured as serial data output signal. Used as data pin 1 in quad-data and dual-data transfers.	I/O

Table 27. LPSPI1 signal descriptions

Chip signal name	Module signal name	Description	I/O
SPI1_SCK	SCK	Serial clock. Input in slave mode, output in master mode.	I/O
SPI1_PCS0	PCS[0]	Peripheral Chip Select. Input in slave mode, output in master mode.	I/O
SPI1_PCS1	PCS[1]	Peripheral Chip Select or Host Request. Host Request pin is selected when HREN=1 and HRSEL=0. Input in either slave mode or when used as Host Request, output in master mode.	I/O
SPI1_PCS2	PCS[2]	Peripheral Chip Select or data pin 2 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O
SPI1_PCS3	PCS[3]	Peripheral Chip Select or data pin 3 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O
SPI1_SOUT	SOUT	Serial Data Output. Can be configured as serial data input signal. Used as data pin 0 in quad-data and dual-data transfers.	I/O
SPI1_SIN	SIN	Serial Data Input. Can be configured as serial data output signal. Used as data pin 1 in quad-data and dual-data transfers.	I/O

Table 28. LPSPI2 signal descriptions

Chip signal name	Module signal name	Description	I/O
SPI2_SCK	SCK	Serial clock. Input in slave mode, output in master mode.	I/O
SPI2_PCS0	PCS[0]	Peripheral Chip Select. Input in slave mode, output in master mode.	I/O
SPI2_PCS1	PCS[1]	Peripheral Chip Select or Host Request. Host Request pin is selected when HREN=1 and HRSEL=0. Input in either slave mode or when used as Host Request, output in master mode.	I/O
SPI2_PCS2	PCS[2]	Peripheral Chip Select or data pin 2 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O

Table continues on the next page...

Table 28. LPSPI2 signal descriptions (continued)

Chip signal name	Module signal name	Description	I/O
SPI2_PCS3	PCS[3]	Peripheral Chip Select or data pin 3 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O
SPI2_SOUT	SOUT	Serial Data Output. Can be configured as serial data input signal. Used as data pin 0 in quad-data and dual-data transfers.	I/O
SPI2_SIN	SIN	Serial Data Input. Can be configured as serial data output signal. Used as data pin 1 in quad-data and dual-data transfers.	I/O

Table 29. LPSPI3 signal descriptions

Chip signal name	Module signal name	Description	I/O
SPI3_SCK	SCK	Serial clock. Input in slave mode, output in master mode.	I/O
SPI3_PCS0	PCS[0]	Peripheral Chip Select. Input in slave mode, output in master mode.	I/O
SPI3_PCS1	PCS[1]	Peripheral Chip Select or Host Request. Host Request pin is selected when HREN=1 and HRSEL=0. Input in either slave mode or when used as Host Request, output in master mode.	I/O
SPI3_PCS2	PCS[2]	Peripheral Chip Select or data pin 2 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O
SPI3_PCS3	PCS[3]	Peripheral Chip Select or data pin 3 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O
SPI3_SOUT	SOUT	Serial Data Output. Can be configured as serial data input signal. Used as data pin 0 in quad-data and dual-data transfers.	I/O
SPI3_SIN	SIN	Serial Data Input. Can be configured as serial data output signal. Used as data pin 1 in quad-data and dual-data transfers.	I/O

Table 30. LPI2C0 signal descriptions

Chip signal name	Module signal name	Description	I/O
I2C0_SCL	SCL	LPI2C clock line. In 4-wire mode, this is the SCL input pin.	I/O
I2C0_SDA	SDA	LPI2C data line. In 4-wire mode, this is the SDA input pin.	I/O
LPI2C0_HREQ	HREQ	Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle.	I
LPI2C0_SCLS	SCLS	Secondary I2C clock line. In 4-wire mode, this is the SCLS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SCL pin.	I/O
LPI2C0_SDAS	SDAS	Secondary I2C data line. In 4-wire mode, this is the SDAS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SDA pin.	I/O

Table 31. LPI2C1 signal descriptions

Chip signal name	Module signal name	Description	I/O
I2C1_SCL	SCL	LPI2C clock line. In 4-wire mode, this is the SCL input pin.	I/O
I2C1_SDA	SDA	LPI2C data line. In 4-wire mode, this is the SDA input pin.	I/O
LPI2C1_HREQ	HREQ	Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle.	I
LPI2C1_SCLS	SCLS	Secondary I2C clock line. In 4-wire mode, this is the SCLS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SCL pin.	I/O
LPI2C1_SDAS	SDAS	Secondary I2C data line. In 4-wire mode, this is the SDAS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SDA pin.	I/O

Table 32. LPI2C2 signal descriptions

Chip signal name	Module signal name	Description	I/O
I2C2_SCL	SCL	LPI2C clock line. In 4-wire mode, this is the SCL input pin.	I/O
I2C2_SDA	SDA	LPI2C data line. In 4-wire mode, this is the SDA input pin.	I/O
LPI2C2_HREQ	HREQ	Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle.	I
LPI2C2_SCLS	SCLS	Secondary I2C clock line. In 4-wire mode, this is the SCLS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SCL pin.	I/O
LPI2C2_SDAS	SDAS	Secondary I2C data line. In 4-wire mode, this is the SDAS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SDA pin.	I/O

Table 33. LPI2C3 signal descriptions

Chip signal name	Module signal name	Description	I/O
I2C3_SCL	SCL	LPI2C clock line. In 4-wire mode, this is the SCL input pin.	I/O
I2C3_SDA	SDA	LPI2C data line. In 4-wire mode, this is the SDA input pin.	I/O
LPI2C3_HREQ	HREQ	Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle.	I
LPI2C3_SCLS	SCLS	Secondary I2C clock line. In 4-wire mode, this is the SCLS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SCL pin.	I/O
LPI2C3_SDAS	SDAS	Secondary I2C data line. In 4-wire mode, this is the SDAS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SDA pin.	I/O

Table 34. LPUART0 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPUART0_CTS	CTS	Clear to Send.	I
LPUART0_RTS	RTS	Request to send.	O
LPUART0_TX	TXD	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
LPUART0_RX	RXD	Receive data.	I

Table 35. LPUART1 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPUART1_CTS	CTS	Clear to Send.	I
LPUART1_RTS	RTS	Request to send.	O
LPUART1_TX	TXD	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
LPUART1_RX	RXD	Receive data.	I

Table 36. LPUART2 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPUART2_CTS	CTS	Clear to Send.	I
LPUART2_RTS	RTS	Request to send.	O
LPUART2_TX	TXD	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
LPUART2_RX	RXD	Receive data.	I

Table 37. LPUART3 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPUART3_CTS	CTS	Clear to Send.	I
LPUART3_RTS	RTS	Request to send.	O
LPUART3_TX	TXD	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
LPUART3_RX	RXD	Receive data.	I

Table 38. SDHC signal descriptions

Chip signal name	Module signal name	Description	I/O
SDHC0_DCLK	CLK	Clock for MMC/SD/SDIO card	O
SDHC0_CMD	CMD	CMD line connect to card	I/O
SDHC0_D0	DAT0	DAT0 line in all modes. Also used to detect busy state	I/O
SDHC0_D1	DAT1	DAT1 line in 4/8-bit mode.Also used to detect interrupt in 1/4-bit mode	I/O
SDHC0_D2	DAT2	DAT2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	I/O
SDHC0_D3	DAT3	DAT3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode	I/O
SDHC0_D4	DAT4	DAT4 line in 8-bit mode. Not used in other modes	I/O
SDHC0_D5	DAT5	DAT5 line in 8-bit mode. Not used in other modes	I/O
SDHC0_D6	DAT6	DAT6 line in 8-bit mode. Not used in other modes	I/O
SDHC0_D7	DATA7	DAT7 line in 8-bit mode.Not used in other modes	I/O

Table 39. I^2S0 signal descriptions

Chip signal name	Module signal name	Description	I/O
I2S0_TX_BCLK	SAI_TX_BCLK	Transmit Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
I2S0_TX_FS	SAI_TX_SYNC	Transmit Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
I2S0_TX_Dn n=[1:0]	SAI_TX_DATA[1:0]	Transmit Data. The transmit data is generated synchronously by the bit clock and is tristated whenever not transmitting a word.	O
I2S0_RX_BCLK	SAI_RX_BCLK	Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
I2S0_RX_FS	SAI_RX_SYNC	Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
I2S0_RX_Dn	SAI_RX_DATA[1:0]	Receive Data. The receive data is sampled synchronously by the bit clock.	I
I2S0_MCLK	MCLK_EN	Audio Master Clock.	I

Table 40. FlexIO signal descriptions

Chip signal name	Module signal name	Description	I/O
FXIO0_Dn (n=[31:0]	FXIO_Dn (n=[31:0]	Bidirectional FlexIO Shifter and Timer pin inputs/outputs	I/O

3.3.6 Analog

Table 41. LPADC0 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPADC0_SE[23:0]	CHnA (n=[23:0]	A-side Analog Channel Inputs	I
VDDA	VDDA	Analog Power Supply	I
VSSA	VSSA	Analog Ground	I

Table 42. LPCMP0 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPCMP0_IN[5:0]	IN[5:0]	Analog voltage inputs	I
LPCMP0_OUT	CMPO	Comparator output	O

Table 43. LPCMP1 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPCMP1_IN[5:0]	IN[5:0]	Analog voltage inputs	I
LPCMP1_OUT	CMPO	Comparator output	O

Table 44. LPDAC0 signal descriptions

Chip signal name	Module signal name	Description	I/O
DAC0_OUT	—	DAC output	O

Table 45. VREF signal descriptions

Chip signal name	Module signal name	Description	I/O
VREF_OUT	VREF_OUT	Internally-generated Voltage Reference output	O

3.3.7 Human-machine interfaces (HMI)

Table 46. GPIO signal descriptions

Chip signal name	Module signal name	Description	I/O
PTA[31:0][1]	PORTA31–PORTA0	General-purpose input/output	I/O
PTB[31:0][1]	PORTB31–PORTB0	General-purpose input/output	I/O
PTC[31:0][1]	PORTC31–PORTC0	General-purpose input/output	I/O
PTD[31:0][1]	PORTD31–PORTD0	General-purpose input/output	I/O
PTE[31:0][1]	PORTE31–PORTE0	General-purpose input/output	I/O

1. The available GPIO pins depends on the specific package. See the signal multiplexing section for which exact GPIO signals are available.

3.3.8 Timer modules

Table 47. LPTMR0 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR0_ALT[3:1]	LPTMR_ALTn,n=[3:1]	Pulse Counter Input - The LPTMR can select one of the input pins to be used in Pulse Counter mode.	I

Table 48. LPTMR1 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR1_ALT[3:1]	LPTMR_ALTn,n=[3:1]	Pulse Counter Input - The LPTMR can select one of the input pins to be used in Pulse Counter mode.	I

Table 49. LPTMR2 signal descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR2_ALT[3:1]	LPTMR_ALTn,n=[3:1]	Pulse Counter Input - The LPTMR can select one of the input pins to be used in Pulse Counter mode.	I

Table 50. TPM0 signal descriptions

Chip signal name	Module signal name	Description	I/O
TPM0_CH[5:0]	TPM_CHn (n=[5:0])	TPM channel. A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O

Table continues on the next page...

Table 50. TPM0 signal descriptions (continued)

Chip signal name	Module signal name	Description	I/O
TPM0_CLKIN	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the counter on every rising edge synchronized to the counter clock.	I

Table 51. TPM1 signal descriptions

Chip signal name	Module signal name	Description	I/O
TPM1_CH[1:0]	TPM_CHn (n=[1:0])	TPM channel. A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O
TPM1_CLKIN	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the counter on every rising edge synchronized to the counter clock.	I

Table 52. TPM2 signal descriptions

Chip signal name	Module signal name	Description	I/O
TPM2_CH[5:0]	TPM_CHn (n=[5:0])	TPM channel. A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O
TPM2_CLKIN	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the counter on every rising edge synchronized to the counter clock.	I

Table 53. TPM3 signal descriptions

Chip signal name	Module signal name	Description	I/O
TPM3_CH[1:0]	TPM_CHn (n=[1:0])	TPM channel. A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O
TPM3_CLKIN	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the counter on every rising edge synchronized to the counter clock.	I

Table 54. RTC signal descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL32	EXTAL32	32.768 kHz oscillator input	I

Table continues on the next page...

Table 54. RTC signal descriptions (continued)

Chip signal name	Module signal name	Description	I/O
XTAL32	XTAL32	32.768 kHz oscillator output	O
RTC_CLKOUT	RTC_CLKOUT	Prescaler square-wave output or 32kHz crystal clock	O
RTC_WAKEUP_b	$\overline{\text{RTC\_WAKEUP}}$	Active low wakeup for external device	O

3.3.9 Security modules

Table 55. Tamper detect signal descriptions

Chip signal name	Module signal name	Description	I/O
TAMPER[3:0] [1]	RTC_TAMPER[3:0]	Tamper pin input	I

1. The TAMPER signals have dedicated pins and are not included in the JTAG boundary scan. TAMPER0 is an exception because it is priority muxed with the RTC_WAKEUP_b function. If TAMPER0 is enabled as either an input or output, the RTC_WAKEUP_b function is disabled. The RTC_WAKEUP_b pin can be configured to assert on a Tamper Detect, if the RTC enables the DryIce tamper detect interrupt.

3.4 Pinouts diagram

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17A	
	PTA30/ LLWU_P3	PTA28	PTA27	NC	PTA26	NC	PTA15	NC	PTA10	NC	NC	NC	VSS	NC	NC	VSS	VSS	A
B	PTB2/ LLWU_P5	PTA30/ LLWU_P3	PTB0	NC	PTA25	PTA22/ LLWU_P2	PTA21	NC	PTA4	PTA0	NC	NC	NC	VSS	VSS	VSS	NC	B
C	PTB3	PTB4/ LLWU_P6	PTB1/ LLWU_P4	PTA31	VSS	NC	PTA20	NC	VDDIO1	NC	NC	NC	VSS	NC	VSS	VSS	NC	C
D	NC	PTB5	NC	NC	VSS	PTA24	PTA19	PTA18	VSS	NC	PTA3	RESET_b	VDDIO2	NC	VSS	NC	NC	D
E	PTB6/LL WU_P7	PTB7/LL WU_P8	VDDIO1	VDDIO1	NC	PTA23	NC	PTA14	NC	PTA9	NC	PTA1/ LLWU_P0	NC	VSS	VSS	EXTAL32	XTAL32	E
F	NC	NC	NC	PTB9	PTB8/ LLWU_P9	NC	PTA17	NC	NC	NC	PTA2/ LLWU_P1	NC	TAMPER1/ RTC_CLKOUT	TAMPER0 RTC_WAKEUP	NC	VSS	NC	F
G	PTB15	PTB14	PTB13	PTB12	NC	PTB11	NC	NC	NC	NC	NC	TAMPER2	NC	PTE28	PTE29	VBAT	PTE30	G
H	NC	PTB18	NC	NC	PTB16/ LLWU_P10	NC	NC	VSS	VDD_CORE	VSS	NC	NC	TAMPER3	PTE27	NC	NC	NC	H
J	PTB20 LLWU_P11	PTB21	VDDIO1	VSS	NC	NC	NC	VDD_CORE	NC	VDDIO1	NC	NC	NC	VSS	VDDIO2	PTE22	PTE21	J
K	NC	NC	NC	PTB19	PTB17	NC	NC	VSS	VDDIO1	VSS	NC	NC	PTE18	NC	NC	PTE19	NC	K
L	PTB22/LL WU_P12	PTB24	PTB29	PTB26	NC	PTB25/LL WU_P13	NC	NC	NC	NC	NC	PTE12/LL WU_P26	NC	PTE16	PTE17	PTE14	PTE15	L
M	NC	PTC1	NC	PTB28/LL WU_P14	PTB30	NC	PTB31	NC	NC	NC	PTE4	NC	PTE10/LL WU_P25	PTE11	NC	NC	NC	M
N	PTC0	PTC7/ LLWU_P15	VSS	USB0_VSS	NT	PTC29	NT	PTD4	NT	PTD5	NT	PTE3/ LLWU_P22	NT	VDD_CORE	VDD_CORE	PTE9/ LLWU_P24	PTE13	N
P	NC	NC	PTC8	NC	VDDIO1	PTC27	PTD1	NC	VSS	PTD7	PTD10/LL WU_P20	PTE2	VSS	NC	NC	PTE8/ LLWU_P23	NC	P
R	PTC9/ LLWU_P16	PTC10	PTC12/LL WU_P18	NC	VDDIO1	NC	PTC30	NC	VDDIO1	NC	PTD11	NC	VSS	PTE0	VSSA	PTE1/ LLWU_P21	PTE5	R
T	PTC11/LL WU_P17	VDD_DCDC	VOUT_AUX	LN	VOUT_CORE	NC	PTD0	PTD3	PTD8/ LLWU_P19	NC	USB0_DP	USB0_DM	VOUT33	NC	VREF_OUT	VSSA	DAC0_OUT	T
U	VDD_DCDC	LP	GND	NC	PTC28	NC	PTD2	NC	PTD6	NC	PTD9	NC	VREGIN	NC	VDDA	VREFH	VREFL	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 7. VFBGA Pinout Diagram

3.5 Package dimensions

The following figures show the dimensions of the package options for the devices supported by this document.

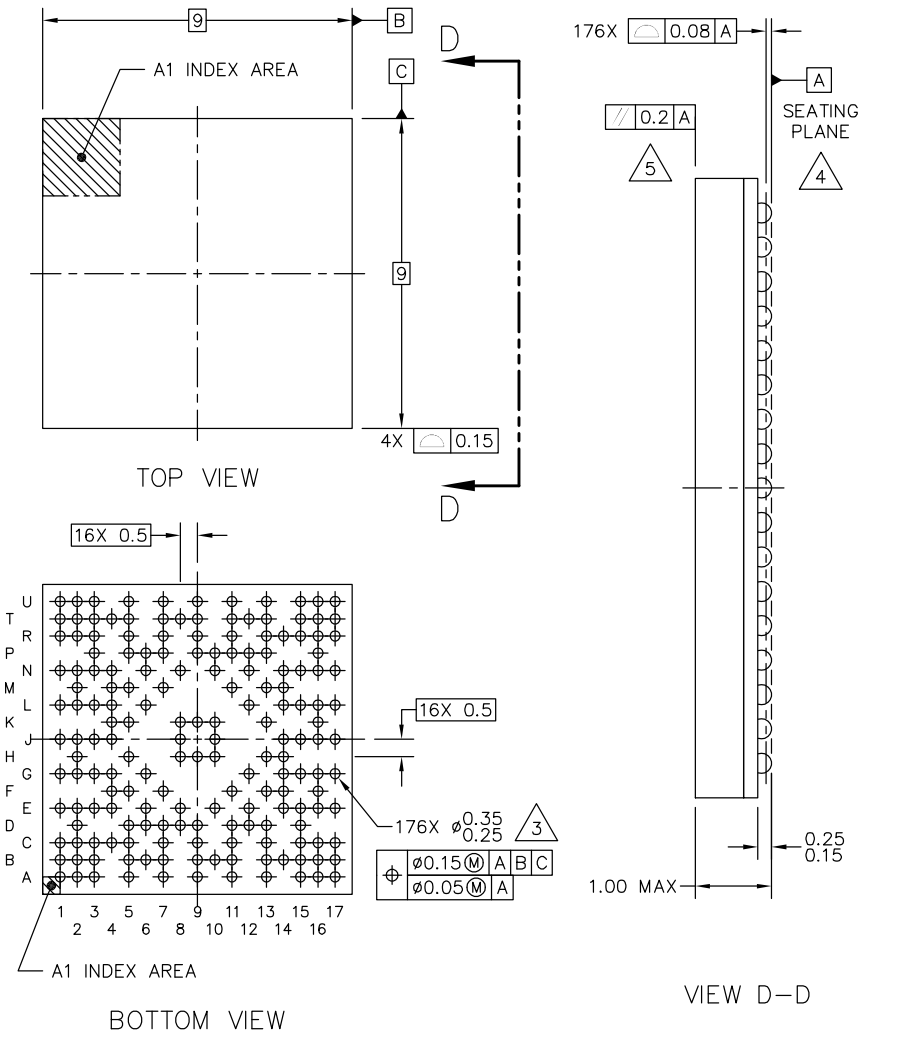


Figure 8. 176 VFBGA package dimension

4 Electrical characteristics

4.1 Terminology and guidelines

4.1.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. **NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

4.1.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

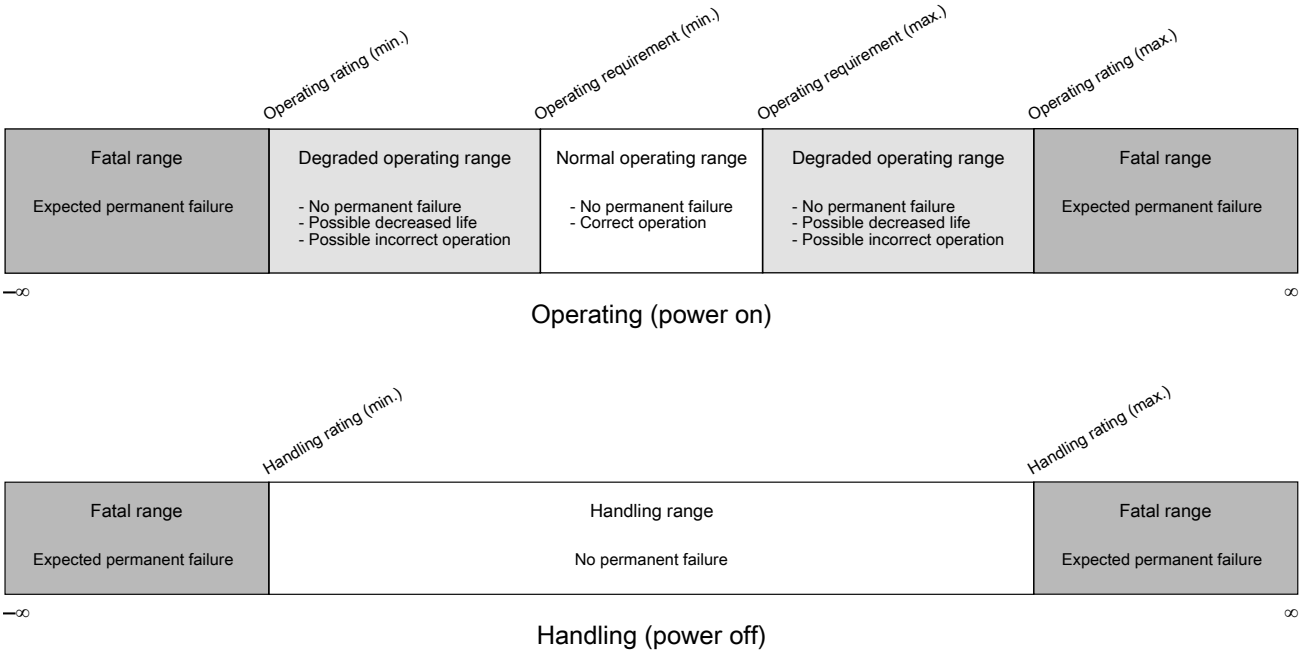
EXAMPLE

4.1.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DDIOx}	Supply voltage	3.3	V

4.1.4 Relationship between ratings and operating requirements



4.1.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

4.2 Ratings

4.2.1 Thermal handling ratings

Table 56. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.

2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2.2 Moisture handling ratings

Table 57. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2.3 ESD handling ratings

Table 58. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.2.4 Voltage and current operating ratings

Table 59. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit	Note
V_{DD_DCDC}	MCU regulator input	-0.3	3.6	V	
V_{DDIOx}	Digital supply voltage	-0.3	3.6	V	
V_{DD_CORE}	Internal digital logic supply voltage	-0.3	1.47	V	
V_{DDA}	Analog supply voltage	V_{DDIO} - 0.3	V_{DDIO} + 0.3	V	1
V_{BAT}	RTC supply voltage	-0.3	3.6	V	
I_{DD}	Digital supply current	—	120	mA	
V_{IO}	IO pin input voltage	-0.3	V_{DDIOx} + 0.3	V	
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA	

Table continues on the next page...

Table 59. Voltage and current operating ratings (continued)

Symbol	Description	Min.	Max.	Unit	Note
V_{USB_DP}	USB_DP input voltage	-0.3	3.63	V	
V_{USB_DM}	USB_DM input voltage	-0.3	3.63	V	
V_{REGIN}	USB regulator input	-0.3	6	V	

1. The V_{DDIO} here is the Maximum of V_{DDIO1} and V_{DDIO2}.

4.2.4.1 Required Power-On-Reset (POR) Sequencing

- V_{DDIO1} and V_{DD_CORE}

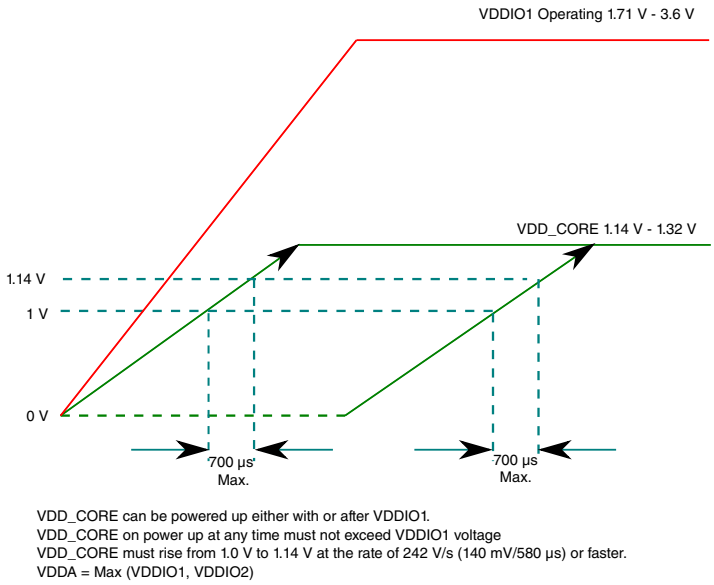
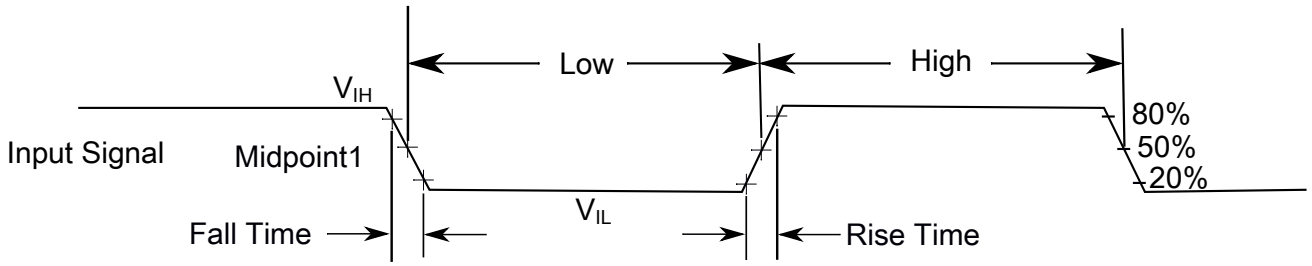


Figure 9. V_{DD_CORE}/ V_{DDIO1} Powering sequence

4.3 General

4.3.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + (V_{IH} - V_{IL}) / 2

Figure 10. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L=30 pF loads
- Slew rate disabled
- Normal drive strength

4.3.2 Nonswitching electrical specifications

4.3.2.1 Voltage and current operating requirements

NOTE

The term 'V_{DDIO}' in the following table refers to the associated supply rail (either V_{DDIO1} or V_{DDIO2}) of an input or output.

Table 60. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD_DCDC}(RUN)	Supply of DCDC and AUXREG.	2.1	3.6	V	
V_{DD_CORE}(RUN)	Core and digital logic supply voltage for RUN mode	1.14	1.32	V	1
V_{DD_CORE}(HSRUN)	Core and digital logic supply voltage for HSRUN mode	1.33	1.47	V	
V_{DDIO1}	Supply for Ports A, B, C, D and CORELDO	1.71	3.6	V	
V_{DDIO2}	Supply for Port E	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DDIO} - V_{DDA}$	V_{DDIO}-to-V_{DDA} differential voltage	–100	100	mV	2
$V_{SS} - V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{IH}	Input high voltage				

Table continues on the next page...

Table 60. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• 2.7 V ≤ V_{DDIO} ≤ 3.6 V	0.7 × V_{DDIO}	—	V	
	• 1.71 V ≤ V_{DDIO} ≤ 2.7 V	0.75 × V_{DDIO}	—	V	
V_{IL}	Input low voltage				
	• 2.7 V ≤ V_{DDIO} ≤ 3.6 V	—	0.35 × V_{DDIO}	V	
	• 1.71 V ≤ V_{DDIO} ≤ 2.7 V	—	0.3 × V_{DDIO}	V	
V_{HYS}	Input hysteresis	0.06 × V_{DDIO}	—	V	
I_{ICIO}	IO pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-5	—	mA	3
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DDIO}	V_{DDIO}	V	4
V_{RAM}	V_{DD_CORE} voltage required to retain RAM	1.14	—	V	

1. The cores will still execute code in RUN if the core voltage is greater than 1.32 V. However full chip functionality is not guaranteed when in RUN mode and the core voltage is greater than 1.32 V. The core voltage must only be elevated to greater than 1.32 V when transitioning to HSRUN mode.
2. The V_{DDIO} here is the Maximum of V_{DDIO1} and V_{DDIO2}
3. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to the corresponding V_{DDIO} supply. If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|.
4. Open drain outputs must be pulled to whichever supply voltage corresponds to that IO, either VDDIO1 or VDDIO2 as appropriate.

4.3.2.2 HVD, LVD and POR operating requirements

Table 61. V_{DDIO1} supply HVD, LVD and POR Operating Ratings

Characteristic	Symbol	Min	Typ	Max	Unit
High Voltage Detect (High Trip Point)	V_{HVDH}	—	3.72	—	V
High Voltage Detect (Low Trip Point)	V_{HVDL}	—	3.46	—	V
POR re-arm voltage	V_{POR}	0.8	1.1	1.5	V
Falling low-voltage detect threshold -- high range (LVDV=01)	V_{LVDH}	2.48	2.56	2.64	V
Low-voltage warning thresholds -- high range Level 1 falling (LVWV=00) Level 2 falling (LVWV=01)	 V_{LVW1} V_{LVW2}	 2.62 2.72	 2.70 2.80	 2.78 2.88	V

Table continues on the next page...

Table 61. V_{DDIO1} supply HVD, LVD and POR Operating Ratings (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Low-voltage inhibit reset/recover hysteresis -- high range	V_{HYS}	—	60	—	mV
Falling low-voltage detect threshold -- low range (LVDV=00)	V_{LVDL}	1.54	1.60	1.66	V
Low-voltage warning thresholds -- low range Level 1 falling (LVWV=00) Level 2 falling (LVWV=01)	 V_{LVW1} V_{LVW2}	 1.74 1.84	 1.80 1.90	 1.86 1.96	V
Low-voltage inhibit reset/recover hysteresis -- low range	V_{HYS}	—	40	—	mV
Bandgap voltage reference voltage	V_{BG}	0.97	1.00	1.03	V

NOTE

There is no LVD circuit for VDDIO2 domain

Table 62. Low Voltage Detect of V_{DD_CORE} supply

Characteristic	Symbol	Min	Typ	Max	Unit
Low Voltage Detect of V_{DD_CORE} supply[1]	$V_{LVD\_VDD\_CORE}$	0.95	1	1.08	V

1. There is no High Voltage Detect on V_{DD_CORE}

4.3.2.3 Voltage and current operating behaviors

NOTE

The term 'V_{DDIO}' in the following table refers to the associated supply rail (either V_{DDIO1} or V_{DDIO2}) of an input or output.

Table 63. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad • 2.7 V ≤ V_{DDIO} ≤ 3.6 V, I_{OH} = –5 mA • 1.71 V ≤ V_{DDIO} ≤ 2.7 V, I_{OH} = –2.5 mA	 V_{DDIO} – 0.5 V_{DDIO} – 0.5		 — —	 V V	1
V_{OH}	Output high voltage — High drive pad • 2.7 V ≤ V_{DDIO} ≤ 3.6 V, I_{OH} = –20 mA • 1.71 V ≤ V_{DDIO} ≤ 2.7 V, I_{OH} = –10 mA	 V_{DDIO} – 0.5 V_{DDIO} – 0.5		 — —	 V V	1

Table continues on the next page...

Table 63. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{OHT}	Output high current total for all ports	—		100	mA	
V_{OL}	Output low voltage — Normal drive pad • 2.7 V ≤ V_{DDIO} ≤ 3.6 V, I_{OL} = 5 mA • 1.71 V ≤ V_{DDIO} ≤ 2.7 V, I_{OL} = 2.5 mA	 — —		 0.5 0.5	 V V	1
V_{OL}	Output low voltage — High drive pad • 2.7 V ≤ V_{DDIO} ≤ 3.6 V, I_{OL} = 20 mA • 1.71 V ≤ V_{DDIO} ≤ 2.7 V, I_{OL} = 10 mA	 — —		 0.5 0.5	 V V	1
I_{OLT}	Output low current total for all ports	—		100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—		1	µA	2
I_{IN}	Input leakage current (per pin) at 25 °C	—		0.025	µA	2
I_{IN}	Input leakage current (total all pins) for full temperature range	—		41	µA	2
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—		1	µA	
R_{PU}	Internal pullup resistors	20		50	kΩ	3

1. PTC[12:7], PTD[11:8], and PTE[11:10] I/O have both high drive and normal drive capability selected by the associated PORTx_PCRn[DSE] control bit. All other GPIOs are normal drive only. PTD[7:2], PTE[12,9:8,5:1], PTB[2,0] are also fast pins.
2. Measured at V_{DDIO} = 3.6 V
3. Measured at V_{DDIO} supply voltage = V_{DDIO} min and Vinput = V_{SS}

4.3.2.4 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration with only CPU0 in Run mode and CPU1 disabled:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- SCG configured in FIRC mode; peripheral functional clocks from FIRCDIV3_CLK and USB clock from FIRCDIV1_CLK

Table 64. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DDIO1} reaches 1.71 V and V_{DD_CORE} reaches 1.14 V to execution of the first instruction across the operating temperature range of the chip.	—	300	—	µs	1

Table continues on the next page...

Table 64. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• VLLS0/VLLS1 → RUN	—	272	353.6	µs	
	• VLLS2/VLLS3 → RUN	—	13.1	17.0	µs	
	• LLS → RUN	—	7.2	9.4	µs	
	• VLPS → RUN	—	3.5	4.6	µs	
	• STOP → RUN	—	3.5	4.6	µs	

1. Normal boot (FTFE_FOPT[BOOT_MODE]=1 and FTFE_FOPT[BOOT_CLK]=1).

4.3.2.5 Power consumption operating behaviors

4.3.2.5.1 Power consumption operating behaviors in regulator mode

The current parameters in the table below are derived from

- code executing a while(1) loop from flash, unless otherwise noted
- Core and system clocks running at 48 MHz, bus and flash clocks running at 24 MHz
- LPFLL at 48 MHz
- VDD_DCDC connected to VDDIO1 and VDDIO2
- Core 0 is CM4 core and core 1 is CM0+ core

Table 65. Power consumption operating behaviors in regulator mode

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)		DCDC (VDD_DCDC=3.3V)		Unit	Notes
				Typ.	Max	Typ.	Max		
I_{DD_DCDC}	Active core in RUN Inactive core in STOP while (1) loop All peripheral clocks disabled Execution from flash	25	0	5.865	6.452	3.492	3.842	mA	
			1	3.410	3.751	2.503	2.753		
			0 & 1	7.397	8.136	4.122	4.535		
		70	0	6.088	6.697	3.629	3.992		
			1	3.592	3.951	2.619	2.881		
			0 & 1	7.675	8.443	4.289	4.718		
		85	0	6.406	7.046	3.786	4.164		
			1	3.813	4.195	2.736	3.009		
			0 & 1	8.069	8.876	4.475	4.923		
		105	0	7.086	7.794	3.068	4.612		

Table continues on the next page...

Table 65. Power consumption operating behaviors in regulator mode (continued)

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)		DCDC (VDD_DCDC=3.3V)		Unit	Notes
				Typ.	Max	Typ.	Max		
			1	4.343	4.777	3.068	3.375		
			0 & 1	8.899	9.789	4.948	5.443		
I_{DD_DCDC}	Active core in RUN Inactive core in STOP while (1) loop All peripheral clocks enabled Execution from flash	25	0	7.536	8.290	4.177	4.595	mA	
			1	4.767	5.244	3.042	3.347		
			0 & 1	10.275	11.302	5.322	5.854		
		70	0	7.770	8.547	4.324	4.756		
			1	4.955	5.450	3.169	3.486		
			0 & 1	10.579	11.637	5.519	6.071		
		85	0	8.094	8.903	4.480	4.928		
			1	5.202	5.722	3.527	3.880		
			0 & 1	10.991	12.090	5.715	6.287		
		105	0	8.784	9.663	4.903	5.393		
			1	5.762	6.338	3.643	4.007		
			0 & 1	11.881	13.070	6.223	6.845		
I_{DD_DCDC}	Active core in RUN Inactive core in STOP while (1) loop Compute Operation Execution from flash	25	0	5.246	5.771	3.199	3.519	mA	
			1	2.822	3.104	2.230	2.453		
			0 & 1	6.663	7.329	3.779	4.157		
		70	0	5.459	6.005	3.335	3.669		
			1	2.988	3.286	2.336	2.569		
			0 & 1	6.941	7.636	3.940	4.334		
		85	0	5.776	6.354	3.487	3.836		
			1	3.219	3.541	2.452	2.697		
			0 & 1	7.330	8.063	4.122	4.534		
		105	0	6.451	7.096	3.884	4.272		
			1	3.743	4.118	2.784	3.063		
			0 & 1	8.160	8.976	4.594	5.053		
I_{DD_DCDC}	Active core in RUN Inactive core in STOP Coremark benchmark code Compute Operation Execution from flash	25	0	5.345	5.879	3.499	3.849	mA	
			1	4.728	5.200	3.000	3.299		
			0 & 1	8.872	9.759	4.874	5.362		
		70	0	5.578	6.135	3.630	3.993		
			1	4.815	5.296	3.110	3.421		
			0 & 1	8.986	9.885	5.050	5.555		
		85	0	6.211	6.832	3.742	4.116		
			1	5.062	5.568	3.107	3.417		
			0 & 1	9.542	10.496	5.0616	5.568		
		105	0	6.711	7.382	4.119	4.531		

Table continues on the next page...

Table 65. Power consumption operating behaviors in regulator mode (continued)

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)		DCDC (VDD_DCDC=3.3V)		Unit	Notes
				Typ.	Max	Typ.	Max		
			1	5.657	6.222	3.444	3.789		
			0 & 1	10.212	11.234	5.654	6.219		
I_{DD_DCDC}	Active core in high speed RUN Inactive core in STOP while (1) loop. All peripheral clocks disabled. Execution from flash Core V_{DD} = 1.4 V. Core clock = 72 MHz	25	0	10.218	11.240	5.975	6.573	mA	
			1	5.338	5.872	3.562	3.919		
			0 & 1	12.814	14.096	7.210	7.931		
		70	0	10.563	11.620	6.183	6.801		
			1	5.660	6.226	3.732	4.105		
			0 & 1	13.199	14.518	7.438	8.182		
		85	0	11.073	12.181	6.425	7.068		
			1	6.118	6.730	3.947	4.342		
			0 & 1	13.691	15.060	7.685	8.454		
		105	0	12.068	13.275	7.053	7.759		
			1	7.087	7.796	4.534	4.988		
			0 & 1	14.687	16.156	8.338	9.172		
I_{DD_DCDC}	Active core in high speed RUN Inactive core in STOP while (1) loop All peripheral clocks enabled Execution from flash Core Vdd = 1.4V Core clock = 72MHz	25	0	12.819	14.101	7.215	7.937	mA	
			1	7.439	8.183	4.512	4.963		
			0 & 1	17.301	19.031	9.420	10.362		
		70	0	13.214	14.535	7.448	8.193		
			1	7.792	8.571	4.712	5.183		
			0 & 1	17.755	19.531	9.703	10.673		
		85	0	13.736	15.109	7.705	8.476		
			1	8.270	9.097	4.932	5.425		
			0 & 1	18.249	20.073	9.975	10.972		
		105	0	14.777	16.255	8.373	9.211		
			1	9.285	10.214	5.554	6.109		
			0 & 1	19.331	21.264	10.688	11.757		
I_{DD_DCDC}	Active core in high speed RUN Inactive core in STOP, Compute Operation Execution from flash Core Vdd = 1.4V Core clock = 72MHz	25	0	9.474	10.422	5.592	6.152	mA	
			1	4.635	5.098	3.205	3.525		
			0 & 1	11.935	13.128	6.752	7.428		
		70	0	9.829	10.812	5.795	6.374		
			1	4.966	5.463	3.373	3.711		
			0 & 1	12.315	13.546	6.980	7.678		
		85	0	10.319	11.350	6.032	6.635		
			1	5.394	5.933	3.584	3.942		
			0 & 1	12.807	14.087	7.226	7.949		
		105	0	11.309	12.440	6.655	7.320		

Table continues on the next page...

Table 65. Power consumption operating behaviors in regulator mode (continued)

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)		DCDC (VDD_DCDC=3.3V)		Unit	Notes
				Typ.	Max	Typ.	Max		
			1	6.363	6.999	4.165	4.582		
			0 & 1	13.813	15.194	7.859	8.645		
I_{DD_DCDC}	Active core in high speed RUN Inactive core in STOP Coremark benchmark code; Execution from flash Core Vdd = 1.4V Core clock = 72MHz	25	0	10.232	11.255	5.963	6.559	mA	
			1	8.033	8.836	4.699	5.169		
			0 & 1	15.751	17.326	8.647	9.512		
		70	0	10.347	11.382	6.265	6.892		
			1	7.881	8.836	4.683	5.152		
			0 & 1	16.036	17.640	9.005	9.905		
		85	0	10.878	11.965	6.352	6.987		
			1	8.394	9.234	5.074	5.581		
			0 & 1	16.714	18.386	8.937	9.830		
		105	0	12.123	13.335	6.979	7.677		
			1	9.735	10.709	5.552	6.108		
			0 & 1	17.831	19.614	9.812	10.793		
I_{DD_DCDC}	Active core in WAIT Inactive core in STOP All peripheral clocks disabled	25	0	2.732	3.005	2.103	2.461	mA	
			1	2.388	2.626	1.103	2.31		
			0 & 1	3.231	3.554	2.43	2.675		
		70	0	2.938	3.232	2.359	2.595		
			1	2.553	2.809	2.214	2.436		
			0 & 1	3.487	3.836	2.579	2.837		
		85	0	3.234	3.557	2.506	2.756		
			1	2.784	3.063	2.326	2.558		
			0 & 1	3.853	4.239	2.746	3.020		
		105	0	3.903	4.332	2.893	3.211		
			1	3.740	3.667	2.653	2.945		
			0 & 1	4.672	5.186	3.203	3.556		
I_{DD_DCDC}	Active core in WAIT Inactive core in STOP All peripheral clocks enabled	25	0	4.398	4.838	2.902	3.193	mA	
			1	3.740	4.114	2.637	3.901		
			0 & 1	6.100	6.710	3.587	3.946		
		70	0	4.610	5.071	3.034	3.337		
			1	3.921	4.313	2.754	3.029		
			0 & 1	6.382	7.021	3.754	4.129		
		85	0	4.917	5.409	3.175	3.493		
			1	4.168	4.585	2.876	3.163		
			0 & 1	6.770	7.447	2.935	4.328		
		105	0	5.587	6.201	3.578	3.972		

Table continues on the next page...

Table 65. Power consumption operating behaviors in regulator mode (continued)

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)		DCDC (VDD_DCDC=3.3V)		Unit	Notes
				Typ.	Max	Typ.	Max		
			1	4.722	5.242	3.223	3.578		
			0 & 1	7.625	8.464	4.423	4.909		
I_{DD_DCDC}	Both cores in PSTOP2 Flash disabled	25	--	1.469	2.423	--	--	mA	
		70	--	1.724	2.879	--	--		
		85	--	2.110	3.481	--	--		
		105	--	2.968	4.779	--	--		
I_{DD_DCDC}	Active core in VLPR Inactive core in VLPS while (1) loop All peripheral clocks disabled Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	0.813	0.894	--	--	mA	
			1	0.448	0.493	--	--		
			0 & 1	1.017	1.118	--	--		
		70	0	0.870	0.957	--	--		
			1	0.498	0.548	--	--		
			0 & 1	1.076	1.184	--	--		
		85	0	0.941	1.036	--	--		
			1	0.570	0.628	--	--		
			0 & 1	1.149	1.264	--	--		
		105	0	1.113	1.224	--	--		
			1	0.741	0.815	--	--		
			0 & 1	1.324	1.457	--	--		
I_{DD_DCDC}	Active core in VLPR Inactive core in VLPS while (1) loop All peripheral clocks enabled Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	1.039	1.143	--	--	mA	
			1	0.638	0.996	--	--		
			0 & 1	1.406	1.5466	--	--		
		70	0	1.097	1.206	--	--		
			1	0.690	1.132	--	--		
			0 & 1	1.467	1.613	--	--		
		85	0	1.174	1.291	--	--		
			1	0.763	1.244	--	--		
			0 & 1	1.539	1.692	--	--		
		105	0	1.344	1.479	--	--		
			1	0.932	1.482	--	--		
			0 & 1	1.714	1.886	--	--		
I_{DD_DCDC}	Active core in VLPR Inactive core in VLPS while (1) loop Compute Operation Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	0.785	0.864	--	--	mA	
			1	0.425	0.663	--	--		
			0 & 1	0.988	1.086	--	--		
		70	0	0.838	0.921	--	--		
			1	0.473	0.776	--	--		
			0 & 1	1.048	1.153	--	--		

Table continues on the next page...

Table 65. Power consumption operating behaviors in regulator mode (continued)

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)		DCDC (VDD_DCDC=3.3V)		Unit	Notes
				Typ.	Max	Typ.	Max		
		85	0	0.916	1.008	--	--		
			1	0.543	0.886	--	--		
			0 & 1	1.124	1.236	--	--		
		105	0	1.084	1.192	--	--		
			1	0.711	1.131	--	--		
			0 & 1	1.294	1.423	--	--		
I_{DD_DCDC}	Active core in VLPR Inactive core in VLPS Coremark benchmark code Compute Operation Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	0.898	0.988	--	--	mA	
			1	0.753	1.175	--	--		
			0 & 1	1.321	1.453	--	--		
		70	0	0.900	0.990	--	--		
			1	0.751	1.231	--	--		
			0 & 1	1.457	1.602	--	--		
		85	0	0.976	1.074	--	--		
			1	0.848	1.382	--	--		
			0 & 1	1.569	1.726	--	--		
		105	0	1.154	1.270	--	--		
			1	1.054	1.676	--	--		
			0 & 1	1.704	1.875	--	--		
I_{DD_DCDC}	Active core in VLPW Inactive core in VLPS All peripheral clocks disabled Flash disabled Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	0.349	0.384	--	--	mA	
			1	0.306	0.477	--	--		
			0 & 1	0.411	0.453	--	--		
		70	0	0.397	0.437	--	--		
			1	0.354	0.580	--	--		
			0 & 1	0.456	0.502	--	--		
		85	0	0.470	0.517	--	--		
			1	0.424	0.692	--	--		
			0 & 1	0.530	0.583	--	--		
		105	0	0.637	0.732	--	--		
			1	0.593	0.942	--	--		
			0 & 1	0.704	0.809	--	--		

4.3.2.5.2 Power consumption operating behaviors in bypass mode

The current parameters in the table below are derived from

- code executing a while(1)
- loop from flash, unless otherwise noted

- Core and system clocks running at 48 MHz, bus and flash clocks running at 24 MHz
- LPFLL at 48MHz
- Core 0 is the CM4 core and core 1 is the CM0+ core

Table 66. Power consumption operating behaviors in bypass mode

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit
				Typ.	Max	Typ.	Max	Typ.	Max	
I_{DD}	Active core in RUN Inactive core in STOP while (1) loop All peripheral clocks disabled Execution from flash	25	0	5.060	5.566	0.194	0.214	0.0000161	0.0000177	mA
			1	2.860	3.1460	0.194	0.214	0.0000148	0.0000163	
			0 & 1	6.365	7.002	0.194	0.214	0.0000162	0.0000179	
		70	0	5.275	5.803	0.200	0.220	0.000209	0.000230	
			1	3.020	3.322	0.200	0.220	0.000210	0.000231	
			0 & 1	6.605	7.266	0.200	0.220	0.000209	0.000230	
		85	0	5.460	6.006	0.204	0.225	0.000476	0.000524	
			1	3.205	3.526	0.204	0.225	0.000474	0.000522	
			0 & 1	6.870	7.557	0.204	0.225	0.000476	0.000524	
		105	0	5.970	6.567	0.214	0.235	0.00138	0.00151	
			1	3.620	3.982	0.214	0.236	0.00137	0.00151	
			0 & 1	7.475	8.223	0.214	0.235	0.00137	0.00151	
I_{DD}	Active core in RUN Inactive core in STOP while (1) loop All peripheral clocks enabled Execution from flash	25	0	6.485	7.134	0.194	0.214	0.0000153	0.0000168	mA
			1	4.090	4.499	0.194	0.214	0.0000151	0.0000166	
			0 & 1	8.685	9.554	0.194	0.213	0.0000154	0.0000170	
		70	0	6.665	7.332	0.200	0.220	0.000210	0.000231	
			1	4.260	4.686	0.200	0.220	0.000209	0.000230	
			0 & 1	8.915	9.807	0.200	0.220	0.000210	0.000231	
		85	0	6.885	7.574	0.204	0.225	0.000474	0.000521	
			1	4.430	4.873	0.204	0.225	0.000473	0.000520	
			0 & 1	9.180	10.098	0.204	0.225	0.000473	0.000520	
		105	0	7.355	8.091	0.214	0.235	0.00137	0.00151	
			1	4.870	5.357	0.214	0.236	0.00137	0.00151	
			0 & 1	9.755	10.731	0.214	0.235	0.00138	0.00151	
I_{DD}	Active core in RUN Inactive core in STOP while (1) loop Compute Operation Execution from flash	25	0	4.570	5.027	0.138	0.152	0.0000151	0.0000166	mA
			1	2.360	2.596	0.138	0.152	0.0000151	0.0000166	
			0 & 1	5.795	6.374	0.138	0.152	0.0000169	0.0000186	
		70	0	4.770	5.247	0.144	0.158	0.000211	0.000232	
			1	2.525	2.778	0.144	0.158	0.000210	0.000231	
			0 & 1	6.035	6.639	0.144	0.158	0.000209	0.000230	
		85	0	4.965	5.462	0.147	0.162	0.000472	0.000520	
			1	2.700	2.970	0.147	0.162	0.000471	0.000518	

Table continues on the next page...

Table 66. Power consumption operating behaviors in bypass mode (continued)

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit
				Typ.	Max	Typ.	Max	Typ.	Max	
			0 & 1	6.290	6.919	0.147	0.162	0.000471	0.000519	
		105	0	5.495	6.045	0.157	0.173	0.00137	0.00150	
			1	3.130	3.443	0.157	0.173	0.00137	0.00151	
			0 & 1	6.910	7.601	0.1567	0.173	0.00138	0.00151	
I_{DD}	Active core in RUN Inactive core in STOP Coremark benchmark code Compute Operation Execution from flash	25	0	5.210	5.731	0.138	0.152	0.0000155	0.0000171	mA
			1	3.820	4.202	0.138	0.152	0.0000145	0.0000160	
			0 & 1	8.330	9.163	0.138	0.152	0.0000142	0.0000156	
		70	0	5.645	6.210	0.144	0.158	0.000210	0.00023152	
			1	4.000	4.400	0.144	0.158	0.000210	0.000231	
			0 & 1	8.730	9.603	0.144	0.158	0.000208	0.000229	
		85	0	5.810	6.391	0.147	0.162	0.000470	0.000517	
			1	4.080	4.488	0.147	0.162	0.000470	0.000517	
			0 & 1	9.095	10.005	0.147	0.162	0.000472	0.000519	
		105	0	6.450	7.095	0.157	0.173	0.00138	0.00151	
			1	4.620	5.082	0.157	0.173	0.00137	0.00151	
			0 & 1	9.710	10.681	0.157	0.173	0.00138	0.00152	
I_{DD}	Active core in high speed RUN Inactive core in STOP while (1) loop All peripheral clocks disabled Execution from flash Core Vdd = 1.4V Core clock = 72MHz	25	0	9.205	10.126	0.534	0.587	0.0000155	0.0000170	mA
			1	4.815	5.297	0.200	0.220	0.0000148	0.0000163	
			0 & 1	11.660	12.826	0.534	0.587	0.0000157	0.0000173	
		70	0	9.545	10.500	0.544	0.598	0.000210	0.000231	
			1	5.160	5.676	0.207	0.228	0.000211	0.000232	
			0 & 1	12.025	13.228	0.544	0.598	0.000211	0.000232	
		85	0	9.880	10.868	0.549	0.604	0.000470	0.000517	
			1	5.515	6.067	0.211	0.232	0.000468	0.000515	
			0 & 1	12.360	13.596	0.549	0.603	0.000474	0.000521	
		105	0	10.720	11.792	0.560	0.616	0.00134	0.00147	
			1	6.355	6.991	0.221	0.243	0.00133	0.00146	
			0 & 1	13.200	14.520	0.560	0.616	0.00134	0.00147	
I_{DD}	Active core in high speed RUN Inactive core in STOP while (1) loop All peripheral clocks enabled Execution from flash Core Vdd = 1.4V Core clock = 72MHz	25	0	11.670	12.837	0.534	0.587	0.0000161	0.0000178	mA
			1	6.850	7.535	0.200	0.220	0.0000154	0.0000169	
			0 & 1	15.885	17.474	0.534	0.587	0.0000159	0.0000175	
		70	0	12.040	13.244	0.544	0.598	0.000212	0.000233	
			1	7.210	7.931	0.207	0.227	0.000211	0.000232	
			0 & 1	16.255	17.881	0.544	0.598	0.000212	0.000233	
		85	0	12.385	13.624	0.549	0.603	0.000470	0.000517	
			1	7.580	8.338	0.211	0.232	0.000472	0.000520	
			0 & 1	16.615	18.277	0.549	0.603	0.000472	0.000519	

Table continues on the next page...

Table 66. Power consumption operating behaviors in bypass mode (continued)

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit
				Typ.	Max	Typ.	Max	Typ.	Max	
		105	0	13.250	14.575	0.560	0.616	0.00134	0.00147	
			1	8.460	9.306	0.221	0.243	0.00134	0.00147	
			0 & 1	17.495	19.245	0.560	0.616	0.00135	0.00148	
I_{DD}	Active core in high speed RUN Inactive core in STOP while (1) loop Compute Operation Execution from flash Core Vdd = 1.4V Core clock = 72MHz	25	0	8.545	9.400	0.478	0.525	0.0000150	0.0000165	mA
			1	4.180	4.598	0.145	0.159	0.0000155	0.0000171	
			0 & 1	10.885	11.974	0.478	0.526	0.0000162	0.0000178	
		70	0	8.885	9.774	0.487	0.536	0.000209	0.000230	
			1	4.525	4.978	0.150	0.165	0.000210	0.000232	
			0 & 1	11.245	12.370	0.488	0.536	0.000211	0.000232	
		85	0	9.220	10.142	0.492	0.541	0.000469	0.000516	
			1	4.880	5.368	0.154	0.169	0.000467	0.000514	
			0 & 1	11.585	12.744	0.492	0.541	0.000470	0.000517	
		105	0	10.080	11.088	0.503	0.553	0.00134	0.00147	
			1	5.725	6.298	0.164	0.180	0.00134	0.00147	
			0 & 1	12.450	13.695	0.503	0.553	0.00134	0.00147	
I_{DD}	Active core in high speed RUN Inactive core in STOP Coremark benchmark code Compute Operation Execution from flash Core Vdd = 1.4V Core clock = 72MHz	25	0	9.725	10.698	0.478	0.526	0.0000153	0.0000168	mA
			1	6.955	7.651	0.144	0.159	0.0000156	0.0000171	
			0 & 1	14.710	16.181	0.478	0.525	0.0000167	0.0000183	
		70	0	9.235	10.159	0.487	0.536	0.000210	0.000231	
			1	7.840	8.624	0.150	0.165	0.000210	0.000231	
			0 & 1	15.015	16.517	0.487	0.536	0.000214	0.000235	
		85	0	9.375	10.313	0.492	0.541	0.000469	0.000516	
			1	7.690	8.459	0.154	0.169	0.000466	0.000513	
			0 & 1	15.305	16.836	0.492	0.541	0.000474	0.000521	
		105	0	11.035	12.139	0.503	0.553	0.00135	0.00148	
			1	9.015	9.917	0.164	0.180	0.00134	0.00147	
			0 & 1	15.620	17.182	0.503	0.553	0.00135	0.00148	
I_{DD}	Active core in WAIT Inactive core in STOP All peripheral clocks disabled	25	0	2.225	2.448	0.194	0.214	0.0000152	0.0000167	mA
			1	1.900	2.090	0.194	0.214	0.0000149	0.0000164	
			0 & 1	2.680	2.948	0.194	0.214	0.0000163	0.0000179	
		70	0	2.435	2.679	0.200	0.220	0.000208	0.000229	
			1	2.060	2.27	0.200	0.220	0.000207	0.000227	
			0 & 1	2.935	3.229	0.200	0.220	0.000209	0.000230	
		85	0	2.645	2.910	0.204	0.225	0.000467	0.000513	
			1	2.225	2.448	0.204	0.225	0.000466	0.000513	
			0 & 1	3.200	3.520	0.204	0.225	0.000465	0.000511	
		105	0	3.190	3.541	0.214	0.238	0.00137	0.00151	

Table continues on the next page...

Table 66. Power consumption operating behaviors in bypass mode (continued)

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit
				Typ.	Max	Typ.	Max	Typ.	Max	
			1	2.665	2.958	0.214	0.238	0.00137	0.00152	
			0 & 1	3.880	4.307	0.214	0.238	0.00137	0.00152	
I_{DD}	Active core in WAIT Inactive core in STOP All peripheral clocks disabled Flash disabled	25	0	3.755	4.131	0.194	0.214	0.0000149	0.0000164	mA
			1	3.155	3.471	0.194	0.214	0.0000158	0.0000173	
			0 & 1	5.245	5.770	0.194	0.214	0.0000158	0.0000173	
		70	0	3.955	4.351	0.200	0.220	0.000209	0.000229	
			1	3.320	3.652	0.200	0.220	0.000210	0.000231	
			0 & 1	5.500	6.050	0.200	0.2200	0.000210	0.000231	
		85	0	4.155	4.571	0.204	0.225	0.000465	0.000512	
			1	3.500	3.850	0.204	0.225	0.000468	0.000515	
			0 & 1	5.745	6.320	0.204	0.225	0.000468	0.000514	
		105	0	4.690	5.206	0.214	0.238	0.00137	0.00152	
			1	3.940	4.373	0.214	0.238	0.00137	0.00152	
			0 & 1	6.405	7.110	0.214	0.237	0.00137	0.00152	
I_{DD}	Both cores in PSTOP2 Flash disabled	25	--	0.695	1.147	0.518	0.855	0.0000153	0.0000252	mA
		70	--	0.961	1.605	0.547	0.913	0.000208	0.000347	
		85	--	1.235	2.038	0.568	0.938	0.000466	0.000768	
		105	--	1.950	3.140	0.621	1.000	0.00137	0.00221	
I_{DD}	Active core in VLPR Inactive core in VLPS while (1) loop All peripheral clocks disabled Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	0.765	0.842	0.0562	0.0618	0.0000131	0.0000144	mA
			1	0.397	0.437	0.0562	0.0618	0.0000145	0.0000159	
			0 & 1	0.967	1.064	0.0562	0.0618	0.0000142	0.0000157	
		70	0	0.820	0.902	0.0597	0.0657	0.000209	0.000229	
			1	0.449	0.494	0.0597	0.0657	0.000207	0.000228	
			0 & 1	1.025	1.128	0.0597	0.0657	0.000208	0.000228	
		85	0	0.874	0.961	0.063	0.0693	0.000471	0.000518	
			1	0.503	0.553	0.0630	0.0693	0.000468	0.000515	
			0 & 1	1.080	1.188	0.0631	0.0694	0.000468	0.000515	
		105	0	1.014	1.115	0.0726	0.0799	0.00136	0.00150	
			1	0.644	0.708	0.0727	0.0799	0.00136	0.00150	
			0 & 1	1.220	1.342	0.0727	0.0799	0.00136	0.00150	
I_{DD}	Active core in VLPR Inactive core in VLPS while (1) loop All peripheral clocks enabled Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	0.990	1.089	0.0562	0.0618	0.0000143	0.0000157	mA
			1	0.590	0.920	0.0562	0.0876	0.0000147	0.0000229	
			0 & 1	1.350	1.485	0.0562	0.0618	0.0000150	0.0000165	
		70	0	1.049	1.154	0.0597	0.0657 1	0.000207	0.000227	
			1	0.643	1.055	0.0597	0.0980	0.000208	0.000342	
			0 & 1	1.410	1.551	0.0597	0.0657	0.000209	0.000230	

Table continues on the next page...

Table 66. Power consumption operating behaviors in bypass mode (continued)

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit
				Typ.	Max	Typ.	Max	Typ.	Max	
		85	0	1.100	1.210	0.0630	0.0693	0.000466	0.000513	
			1	0.697	1.136	0.063	0.103	0.000463	0.000754	
			0 & 1	1.465	1.612	0.0630	0.0693	0.000465	0.000511	
		105	0	1.245	1.370	0.0726	0.0799	0.00136	0.00150	
			1	0.837	1.331	0.073	0.116	0.00136	0.00216	
			0 & 1	1.605	1.766	0.0727	0.0800	0.00137	0.00150	
I_{DD}	Active core in VLPR Inactive core in VLPS while (1) loop Compute Operation Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	0.740	0.813	0.0539	0.0593	0.0000151	0.0000166	mA
			1	0.374	0.583	0.0539	0.0841	0.0000145	0.0000226	
			0 & 1	0.944	1.038	0.0539	0.0593	0.0000155	0.0000170	
		70	0	0.794	0.874	0.0574	0.0632	0.000208	0.000228	
			1	0.427	0.700	0.0574	0.0941	0.000208	0.000341	
			0 & 1	0.998	1.098	0.0574	0.0632	0.000208	0.000229	
		85	0	0.848	0.932	0.0607	0.0667	0.000464	0.000511	
			1	0.480	0.782	0.0607	0.0989	0.000465	0.000758	
			0 & 1	1.057	1.163	0.0607	0.0668	0.000465	0.000511	
		105	0	0.991	1.090	0.0703	0.0773	0.00136	0.00150	
			1	0.621	0.987	0.070	0.112	0.00137	0.00218	
			0 & 1	1.200	1.320	0.0703	0.0773	0.00136	0.00150	
I_{DD}	Active core in VLPR Inactive core in VLPS Coremark benchmark code Compute Operation Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	0.833	0.916	0.0539	0.0593	0.0000145	0.0000160	mA
			1	0.700	1.092	0.0539	0.0841	0.0000151	0.0000235	
			0 & 1	1.390	1.529	0.0539	0.0593	0.0000158	0.0000173	
		70	0	0.859770	0.9457470	0.057415	0.0631565	0.0002069	0.0002276	
			1	0.736	1.206	0.0574	0.0942	0.000207	0.000340	
			0 & 1	1.395	1.535	0.0574	0.0631	0.000207	0.000228	
		85	0	0.907	0.998	0.0607	0.06678	0.000467	0.000513	
			1	0.774	1.261	0.0607	0.0990	0.000468	0.000762	
			0 & 1	1.450	1.595	0.0607	0.0668	0.000464	0.000511	
		105	0	1.100	1.210	0.0703	0.0774	0.00136	0.00150	
			1	0.982	1.562	0.070	0.112	0.00137	0.00217	
			0 & 1	1.670	1.837	0.0704	0.0774	0.00137	0.00150	
I_{DD}	Active core in VLPW Inactive core in VLPS All peripheral clocks disabled Flash disabled Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	0.298	0.328	0.0562	0.0618	0.0000149	0.0000164	mA
			1	0.253	0.395	0.0562	0.0877	0.0000161	0.0000252	
			0 & 1	0.359	0.394	0.0562	0.0618	0.0000154	0.0000169	
		70	0	0.349	0.384	0.0597	0.0657	0.000207	0.000228	
			1	0.304	0.499	0.0597	0.0979	0.000206	0.000339	
			0 & 1	0.410	0.451	0.0598	0.0657	0.000207	0.000227	

Table continues on the next page...

Table 66. Power consumption operating behaviors in bypass mode (continued)

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit
				Typ.	Max	Typ.	Max	Typ.	Max	
		85	0	0.402	0.442	0.0630	0.0693	0.000466	0.000513	
			1	0.357	0.581	0.063	0.103	0.000465	0.000759	
			0 & 1	0.463	0.509	0.0630	0.0693	0.000465	0.000511	
		105	0	0.544	0.626	0.0727	0.0836	0.00137	0.00158	
			1	0.497	0.791	0.073	0.116	0.00137	0.00217	
			0 & 1	0.604	0.695	0.0727	0.0836	0.00137	0.00158	

4.3.2.5.3 Power consumption operating behaviors in low power mode

NOTE

Data for this table was collected in bypass mode except where otherwise noted.

Table 67. Power consumption operating behaviors in low power mode

Symbol	Description[1]		Core		VDDIO1		VDDIO2		Unit	Notes
			Typ.	Max	Typ.	Max	Typ.	Max		
I_{DD_STOP}	Both cores are in STOP mode Core = 1.2V, VDDIO1 = VDDIO2 = 3V	25 °C	12.52	20.66	1.45	2.38	0.015	0.024	µA	
		70 °C	118.01	197.07	4.05	6.76	0.21	0.35		
		85 °C	227.41	375.22	6.85	11.30	0.46	0.76		
		105 °C	517.64	833.40	15.76	25.37	1.36	2.19		
I_{DD_VLPS}	Both cores are in Very Low Power STOP mode Core = 1.2V, VDDIO1 = VDDIO2 = 3V	25 °C	6.05	9.43	1.45	2.26	0.014	0.023	µA	
		70 °C	56.41	92.51	4.11	6.73	0.21	0.34		
		85 °C	109.56	178.58	7.03	11.45	0.47	0.76		
		105 °C	252.07	400.78	16.38	26.04	1.36	2.15		
$I_{DD\_LLS\_NO\_RAM}$	Both cores are in Low Leakage STOP mode, no RAM retained, Core = 1.2V, VDDIO1 = VDDIO2 = 3 V	25 °C	0.54	0.69	1.42	1.78	0.014	0.017	µA	
		70 °C	4.74	6.64	3.80	5.31	0.19	0.27		
		85 °C	9.19	12.68	6.48	8.94	0.44	0.60		
		105 °C	21.43	29.36	14.65	20.07	1.29	1.76		
$I_{DD\_LLS\_ALL\_RAM}$	Both cores are in Low Leakage STOP mode, all RAM retained, Core = 1.2V, VDDIO1 = VDDIO2 = 3V	25 °C	2.29	3.6	1.48	1.8	0.014	0.020	µA	
		70 °C	21.6	39.6	3.88	5.6	0.190	0.274		
		85 °C	42.2	74.2	6.64	9.9	0.440	0.657		
		105 °C	95.9	169.9	15.1	21.1	1.28	1.79		

Table continues on the next page...

Table 67. Power consumption operating behaviors in low power mode (continued)

Symbol	Description[1]		Core		VDDIO1		VDDIO2		Unit	Notes
			Typ.	Max	Typ.	Max	Typ.	Max		
I_{DD_VLLS3}	Both cores are in VLLS3 mode; core = 1.2 V, VDDIO1 = VDDIO2 = 3 V[2]	25 °C	2.38	3.00	1.28	1.61	0.015	0.018	µA	
		70 °C	20.27	28.38	3.64	5.10	0.19	0.27		
		85 °C	39.13	54.00	6.31	8.71	0.43	0.60		
		105 °C	88.77	121.61	14.55	19.93	1.29	1.77		
I_{DD_VLLS1}	Both cores are in VLLS1 mode Core = 1.2V, VDDIO1 = VDDIO2 = 3V[3]	25 °C	0.41	0.52	1.06	1.33	0.014	0.018	µA	
		70 °C	0.70	0.98	3.30	4.62	0.19	0.27		
		85 °C	0.82	1.13	5.89	8.12	0.44	0.60		
		105 °C	1.18	1.62	13.62	18.65	1.29	1.77		

1. The 25 °C data point applies to all valid operating temperatures 25°C and below.
2. ALL RAM Enabled.
3. The following bits were set: CORELPCNFG_ALLREFEN, CORELPCNFG_POREN, CORELPCNFG_LPOEN, CORESC_RTCOVRIDE , CORESC_USBOVRIDE , CORESC_VDDIOOVRIDE.

Table 68. VBAT domain power consumption

Symbol	Descriptions	-40-25 °C		70 °C		85 °C		105 °C		Unit	Notes
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers at 1.8 V	0.59	0.70	1.00	1.30	1.76	2.59	3.00	4.42	µA	1
	Average current when CPU is not accessing RTC registers at 3.0 V	0.71	0.84	1.22	1.59	2.08	3.06	3.50	5.15		

1. VBAT current is measured in the VBAT domain, not core.

Table 69. Peripheral adders — typical value

Symbol	Description	Total at 25 °C	Unit
I_{LPIT}	LPIT peripheral adder measured by placing the device in VLPS mode with using an asynchronous clock source to clock the LPIT. VLPS baseline taken with the clock source enabled, so that load is not included.	0.123	µA
I_{TPM}	TPM peripheral adder measured by placing the device in STOP mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. Clock source used was the SIRC configured for 2 MHz.	5.807	µA
I_{LPTMR}	LPTMR periphera adder measured by placing the device in VLLS1 mode with LPTMR enabled using the LPO.	0.223	µA

Table continues on the next page...

Table 69. Peripheral adders — typical value (continued)

Symbol	Description	Total at 25 °C	Unit
I_{LPUART}	LPUART peripheral adder measured by placing the device in STOP mode with the selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption (2 MHz SIRC).	3.868	µA
I_{LPSPI}	LPSPI peripheral adder for master send mode. Measured by placing the device in Wait mode and using the DMA to initiate continuous transfers to a slave device. This number does not include the DMA adder.	0.293	µA
	LPSPI peripheral adder for slave receive mode. Measured by placing the device in VLPS mode and using the DMA to initiate continuous receptions from a master device. This number does include the DMA adder.	119.335	µA

Table 70. Low power mode RAM adders — typical value

Core	SRAM Array	Start address	End address	Size	25 °C	70 °C	85 °C	105 °C	Unit
CPU0	ITCM0	0x0800_0000	0x0800_1FFF	8 KB	0.027	0.697	0.944	2.504	µA
	ITCM1	0x0800_2000	0x0800_3FFF	8 KB	0.027	0.697	0.944	2.504	µA
	ITCM2	0x0800_4000	0x0800_7FFF	16 KB	0.053	0.991	1.454	3.688	µA
	ITCM3	0x0800_8000	0x0800_FFFF	32 KB	0.110	1.599	2.608	6.229	µA
	DTCM0	0x2000_0000	0x2000_1FFF	8 KB	0.027	0.697	0.944	2.504	µA
	DTCM1	0x2000_2000	0x2000_3FFF	8 KB	0.027	0.697	0.944	2.504	µA
	DTCM2	0x2000_4000	0x2000_7FFF	16 KB	0.053	0.991	1.454	3.688	µA
	DTCM3	0x2000_8000	0x2000_FFFF	32 KB	0.113	1.642	2.726	6.533	µA
	DTCM4	0x2001_0000	0x2001_7FFF	32 KB	0.113	1.642	2.726	6.533	µA
	DTCM5	0x2001_8000	0x2001_FFFF	32 KB	0.113	1.642	2.726	6.533	µA
	DTCM6	0x2002_0000	0x2002_7FFF	32 KB	0.113	1.642	2.726	6.533	µA
	DTCM7	0x2002_8000	0x2002_FFFF	32 KB	0.113	1.642	2.726	6.533	µA
CPU1	TCM0	0x0900_0000	0x0900_1FFF	8 KB	0.027	0.697	0.944	2.504	µA
	TCM1	0x0900_2000	0x0900_3FFF	8 KB	0.027	0.697	0.944	2.504	µA
	TCM2	0x0900_4000	0x0900_7FFF	16 KB	0.053	0.991	1.454	3.688	µA
	TCM3	0x0900_8000	0x0900_FFFF	32 KB	0.113	1.642	2.726	6.533	µA
	TCM4	0x0901_0000	0x0901_7FFF	32 KB	0.113	1.642	2.726	6.533	µA
	TCM5	0x0901_8000	0x0901_FFFF	32 KB	0.113	1.642	2.726	6.533	µA

4.3.2.6 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

4.3.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to nxp.com.
2. Perform a keyword search for “EMC design”.

4.3.2.8 Capacitance attributes

Table 71. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN}	Input capacitance	—	7	pF

4.3.3 Switching specifications

4.3.3.1 Device clock specifications

Table 72. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Run mode[1]
f_{CORE}	Core clock (DIVCORE)	—	72	MHz	High speed run mode
		—	48	MHz	Normal speed run mode
		—	8	MHz	VLPR mode
f_{EXT}	External clock (DIVEXT)	—	72	MHz	High speed run mode
		—	48	MHz	Normal speed run mode
		—	8	MHz	VLPR mode
f_{BUS}	Bus clock (DIVBUS)	—	72	MHz	High speed run mode
		—	48	MHz	Normal speed run mode
		—	8	MHz	VLPR mode
f_{SLOW}	Slow clock (DIVSLOW)	—	24	MHz	High speed run mode
		—	24	MHz	Normal speed run mode

Table continues on the next page...

Table 72. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Run mode[1]
		—	1	MHz	VLPR mode
f_{LLWU}	LLWU clock	—	1	KHz	All modes
f_{WDOG}	WDOG clock	—	24	MHz	High speed run mode and Normal speed run mode
		—	1	MHz	VLPR mode
f_{ADC}	ADC clock	—	48[2]	MHz	High speed run mode and Normal speed run mode
		—	8	MHz	VLPR mode
f_{RTC}	RTC clock	—	32.768	KHz	All modes
f_{TSTMR}	TSTMR clock	—	1	MHz	All modes
f_{LPTMR}	LPTMR clock	—	8	MHz	All modes
f_{TPM}, f_{LPIT}, f_{LPSPI}, f_{LPI2C}, f_{LPUART}, f_{EMVSIM}, f_{I2S}, f_{FLEXIO}	TPM clock, LPIT clock, LPSPI clock, LPI2C clock, LPUART clock, EMVSIM clock, I2S clock, FlexIO clock	—	72	MHz	High speed run mode
		—	48	MHz	Normal speed run mode
		—	8	MHz	VLPR mode
f_{USB}	USB clock	—	48	MHz	High speed run mode and Normal speed run mode
		—	0	MHz	VLPR mode
f_{CAU3}, f_{GPIO}, f_{uSDHC}, f_{TRNG}	CAU3 clock, GPIO clock, uSDHC clock	—	72	MHz	High speed run mode
		—	48	MHz	Normal speed run mode
		—	8	MHz	VLPR mode

1. Normal run mode, High speed run mode, and VLPR mode.
2. See ADC electrical specifications

4.3.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPI2C, and LPUART signals.

NOTE

The term 'V_{DDIO}' in this table refers to the associated supply rail (either V_{DDIO1} or V_{DDIO2}) of an input or output.

Table 73. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise/fall time				
Normal drive pins • $2.7 \le V_{DDIO} \le 3.6$ V • Fast slew rate • Slow slew rate • $1.71 \le V_{DDIO} \le 2.7$ V • Fast slew rate • Slow slew rate	 — — — —	 3 10.5 4 17	 ns	3
High drive pins Normal/low drive enabled • $2.7 \le V_{DDIO} \le 3.6$ V • Fast slew rate • Slow slew rate • $1.71 \le V_{DDIO} \le 2.7$ V • Fast slew rate • Slow slew rate High drive enabled • $2.7 \le V_{DDIO} \le 3.6$ V • Fast slew rate • Slow slew rate • $1.71 \le V_{DDIO} \le 2.7$ V • Fast slew rate • Slow slew rate	 — — — — — — — —	 2.5 10.5 4 17 2 11 2.5 17	 ns	4
Normal drive fast pins • $2.7 \le V_{DDIO} \le 3.6$ V • Fast slew rate • Slow slew rate • $1.71 \le V_{DDIO} \le 2.7$ V • Fast slew rate • Slow slew rate	 — — — —	 0.5 10 0.75 19	 ns	5
High drive fast pins Normal/low drive enabled • $2.7 \le V_{DDIO} \le 3.6$ V	 —	 0.5	 ns	6

Table 73. General switching specifications

Description	Min.	Max.	Unit	Notes
• Fast slew rate • Slow slew rate	—	11		
• 1.71 ≤ V_{DDIO} ≤ 2.7 V • Fast slew rate • Slow slew rate	— —	1 19		
High drive enabled • 2.7 ≤ V_{DDIO} ≤ 3.6 V • Fast slew rate • Slow slew rate	— —	2 13		
• 1.71 ≤ V_{DDIO} ≤ 2.7 V • Fast slew rate • Slow slew rate	— —	4 21		

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. For high drive pins with high drive enabled, load is 75pF; other pins load (normal/low drive) is 25pF. Fast slew rate is enabled by clearing PORTx_PCRn[SRE].
4. High drive pins are PTC[12:7], PTD[11:8], and PTE[11:10]. High drive capability is enabled by setting PORTx_PCRn[DSE].
5. Normal drive fast pins are PTD[7:2], PTE[12,9:8,5:1], PTB[2,0].
6. High drive fast pins are PTC[12:7], PTD[11:8], and PTE[11:10]. High drive capability is enabled by setting PORTx_PCRn[DSE].

NOTE

Only RESET_b pin has analog/passive filter.

4.3.4 Thermal specifications

4.3.4.1 Thermal operating requirements

Table 74. Thermal operating requirements for VFBGA package

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

4.3.4.2 Thermal attributes

Table 75. Thermal attributes

Board type1[1]	Symbol	Description	176 VFBGA	Unit	Notes
JESD51-9,2s2p	$R_{\theta JA}$	Junction to Ambient Thermal Resistance	35.6	°C/W	2, 3
-	Ψ_{JT}	Junction to Package Top Thermal Resistance	0.2	°C/W	4, 3

1. Thermal test board meets JEDEC specification for this package (JESD51-9).
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
3. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the bard, and board construction.
4. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

The thermal characterization parameter (Psi-JT) can be used to determine the junction temperature with a measurement of the temperature at the top of the package case using the following equation:

$T_J = T_T$ + Psi-JT x chip power dissipation

Where T_T is the thermocouple temperature at the top of the package.

4.4 Peripheral operating requirements and behaviors

4.4.1 Core modules

4.4.1.1 Debug trace timing specifications

Table 76. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	1.5	—	ns
T_h	Data hold	1.0	—	ns

4.4.1.2 SWD electricals

Table 77. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

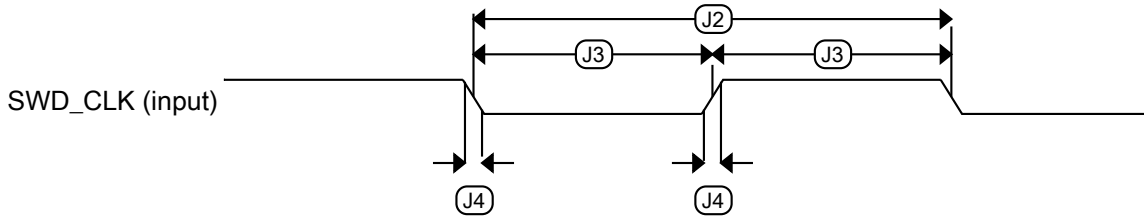


Figure 11. Serial wire clock input timing

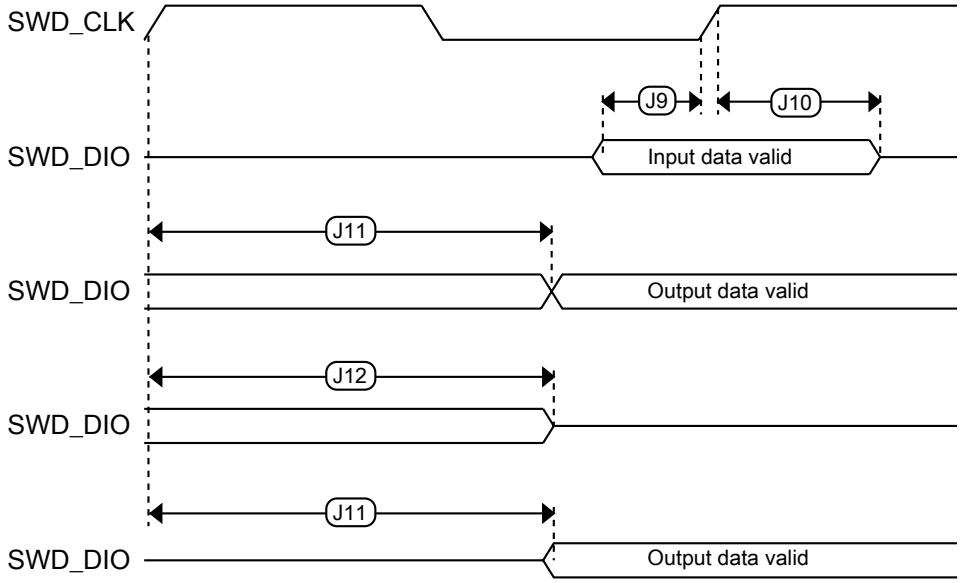


Figure 12. Serial wire data timing

4.4.1.3 JTAG electricals

Table 78. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns

Table continues on the next page...

Table 78. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 79. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	15	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	33	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.4	—	ns
J7	TCLK low to boundary scan output data valid	—	27	ns
J8	TCLK low to boundary scan output high-Z	—	27	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	26.2	ns
J12	TCLK low to TDO high-Z	—	26.2	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

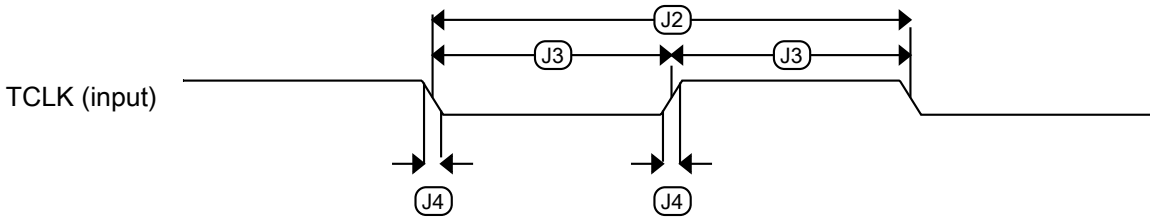


Figure 13. Test clock input timing

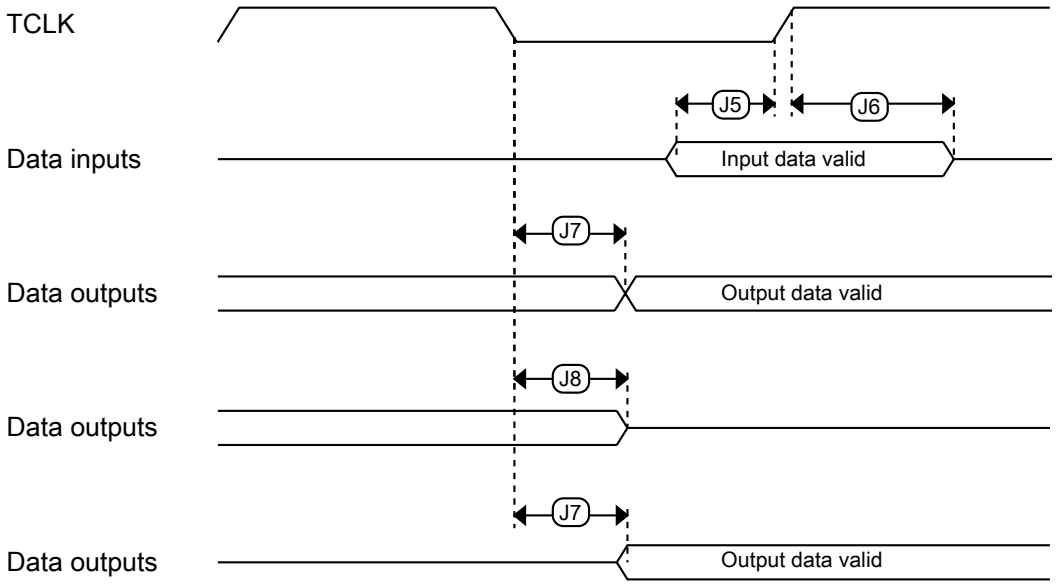


Figure 14. Boundary scan (JTAG) timing

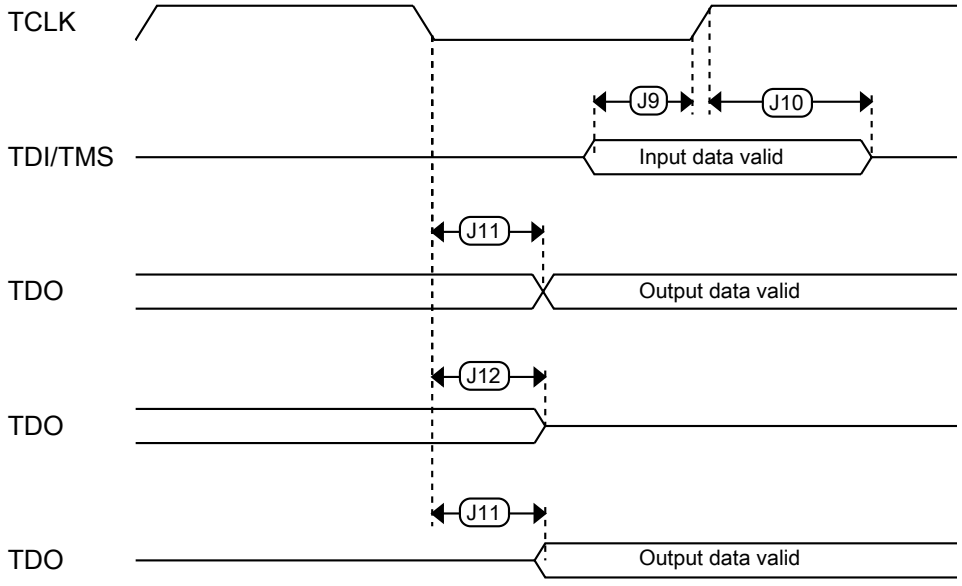


Figure 15. Test Access Port timing

4.4.2 System modules

There are no specifications necessary for the device's system modules.

4.4.3 Clock modules

4.4.3.1 Clock modules

4.4.3.1.1 Fast IRC (FIRC) specifications

Table 80. Fast IRC (FIRC) specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
F_{firc_target}	IRC target frequency (nominal) Trim range = 00 Trim range = 01 Trim range = 10 Trim range = 11	—	 48 52 56 60	—	MHz	1
$\Delta f_{firc\_ol\_lv}$	Open loop total deviation of FIRC frequency at low voltage (VDDIO1=1.71V-1.89V) over full temperature • Regulator disable (SCG_FIRCCSR[FIRCREGOFF]=1) • Regulator enable (SCG_FIRCCSR[FIRCREGOFF]=0)	—	±0.5 ±0.5	±1.5 ±1.5	$\%F_{firc\_target}$	
$\Delta f_{firc\_48M\_ol\_hv}$	Open loop total deviation of FIRC frequency at high voltage (VDDIO1=1.89V-3.6V) over full temperature Regulator enable (SCG_FIRCCSR[FIRCREGOFF]=0)	—	±0.5	±1.0	$\%F_{firc\_target}$	2
$\Delta f_{firc\_60M\_ol\_hv}$	Open loop total deviation of FIRC frequency at high voltage (VDDIO1=1.89V-3.6V) over full temperature Regulator enable (SCG_FIRCCSR[FIRCREGOFF]=0)	—	±0.5	±1.5	$\%F_{firc\_target}$	2
Δf_{firc_cl}	Fine Trim Resolution	—	—	± 0.1	$\%F_{firc\_target}$	
J_{cyc_firc}	Period Jitter (RMS)	—	35	150	ps	
T_{st_firc}	Startup time	—	2	3	µs	3
I_{dd_firc}	Current consumption: • 48 MHz • 52 MHz • 56 MHz • 60 MHz	 — — — —	 350 360 380 400	 400 420 460 500	µA	

1. FIRC trim range is programmable via SCG_FIRCCFG[RANGE].

2. Closed loop operation of the FIRC is only usable for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting FIRC as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_CTRL[CLOCK_RECOVER_EN]=1, SCG_FIRCCSR[FIRCREGOFF]=0).
3. FIRC startup time is defined as the time between clock enablement and clock availability for system use.

4.4.3.1.2 Slow IRC (SIRC) specifications

Table 81. Slow IRC specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_sirc2M}	Supply current in 2 MHz mode	—	14	17	µA	
I_{DD_sirc8M}	Supply current in 8 MHz mode	—	25	35	µA	
f_{sirc}	Output frequency	—	2	—	MHz	1
		—	8	—		
Δf_{sirc}	Total deviation of trimmed frequency over voltage and temperature	—	—	±3.3	$\%f_{sirc}$	
Δf_{sirc_t}	Total deviation of trimmed frequency over voltage and reduced temperature range from -20 ºC to 105 ºC	—	—	3	$\%f_{sirc}$	
T_{su_sirc}	Startup time	—	—	12.5	µs	
J_{cyc_sirc}	Period jitter (RMS) • f_{sirc} = 2 MHz • f_{sirc} = 8 Mhz	— —	350 100	— —	ps	2

1. Selection of output frequency for Slow IRC between 2 MHz and 8 MHz is controlled by SCG_ SIRCCFG[RANGE].
2. This specification was obtained using an NXP developed PCB. Jitter is dependent on the noise characteristics of each PCB and results will vary.

4.4.3.1.3 Low Power Oscillator (LPO) electrical specifications

Table 82. Low Power Oscillator (LPO) electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{LPO}	Internal low power oscillator frequency	0.9	1	1.1	kHz
I_{LPO}	Current consumption	—	8.85	—	µA

4.4.3.1.4 LPFLL electrical specifications

Table 83. LPFLL electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{avg}	Power consumption		240		µA
T_{start}	Start-up time		3.6		µs

Table continues on the next page...

Table 83. LPFLL electrical specifications (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
ΔF_{ol}	Frequency accuracy over temperature and voltage in open loop after process trimmed	–10	—	10	%
ΔF_{cl}	Frequency accuracy in closed loop	–1 [1]	—	1 [1]	%

1. ΔF_{cl} is dependent on reference clock accuracy. For example, if locked to crystal oscillator, ΔF_{cl} is typically limited by trimming ability of the module itself; if locked to other clock source which has 3% accuracy, then ΔF_{cl} can only be ±3%.

4.4.3.2 32 kHz oscillator electrical characteristics

4.4.3.2.1 32 kHz oscillator DC electrical specifications

Table 84. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp} [1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

4.4.3.2.2 32 kHz oscillator frequency specifications

Table 85. 32 kHz Crystal and Oscillator Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Crystal frequency	—	32.768	—	kHz	
T_A	Operating temperature	-40	—	105	°C	1
	Total crystal frequency tolerance	-500	—	500	ppm	2,3
C_L	Load capacitance	—	12.5	—	pF	2
ESR	Equivalent series resistance	—	—	80	kOhms	2
t_{start}	Crystal start-up time	—	1000	—	ms	4

Table continues on the next page...

Table 85. 32 kHz Crystal and Oscillator Specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{ec\_extal32}$	External input clock frequency	—	32.768	—	kHz	5
v_{ec_xtal32}	External input clock amplitude	0.7	—	V_{DD}	V	6

1. Full temperature range of this device. A reduced range can be chosen to meet application needs.
2. Recommended crystal specification.
3. Sum of crystal initial frequency tolerance, crystal frequency stability, and aging tolerances given by crystal vendor.
4. Time from oscillator enable to clock stable. Dependent on the complete hardware configuration of the oscillator.
5. External oscillator connected to EXTAL32K. XTAL32K must be unconnected.
6. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of VSS to VDD.

4.4.4 Memories and memory interfaces

4.4.4.1 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 86. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Frequency of operation	—	24	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	7	ns	
FB3	Address, data, and control output hold	1	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	7.2	—	ns	
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	0	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_BE/BWE}n}$, $\overline{\text{FB\_CS}n}$, $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$, $\overline{\text{FB\_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB\_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB\_TA}}$.

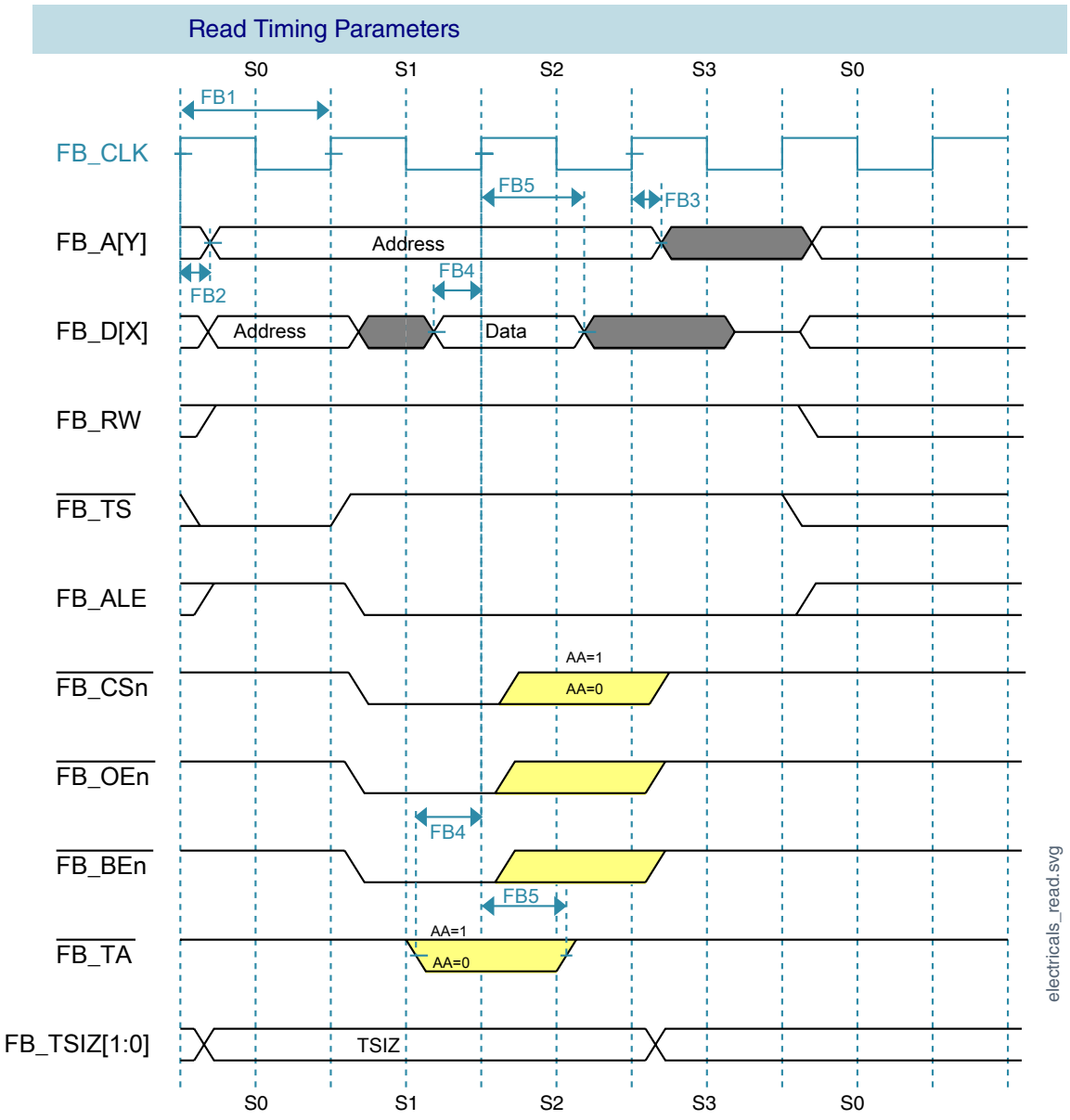


Figure 16. FlexBus read timing diagram

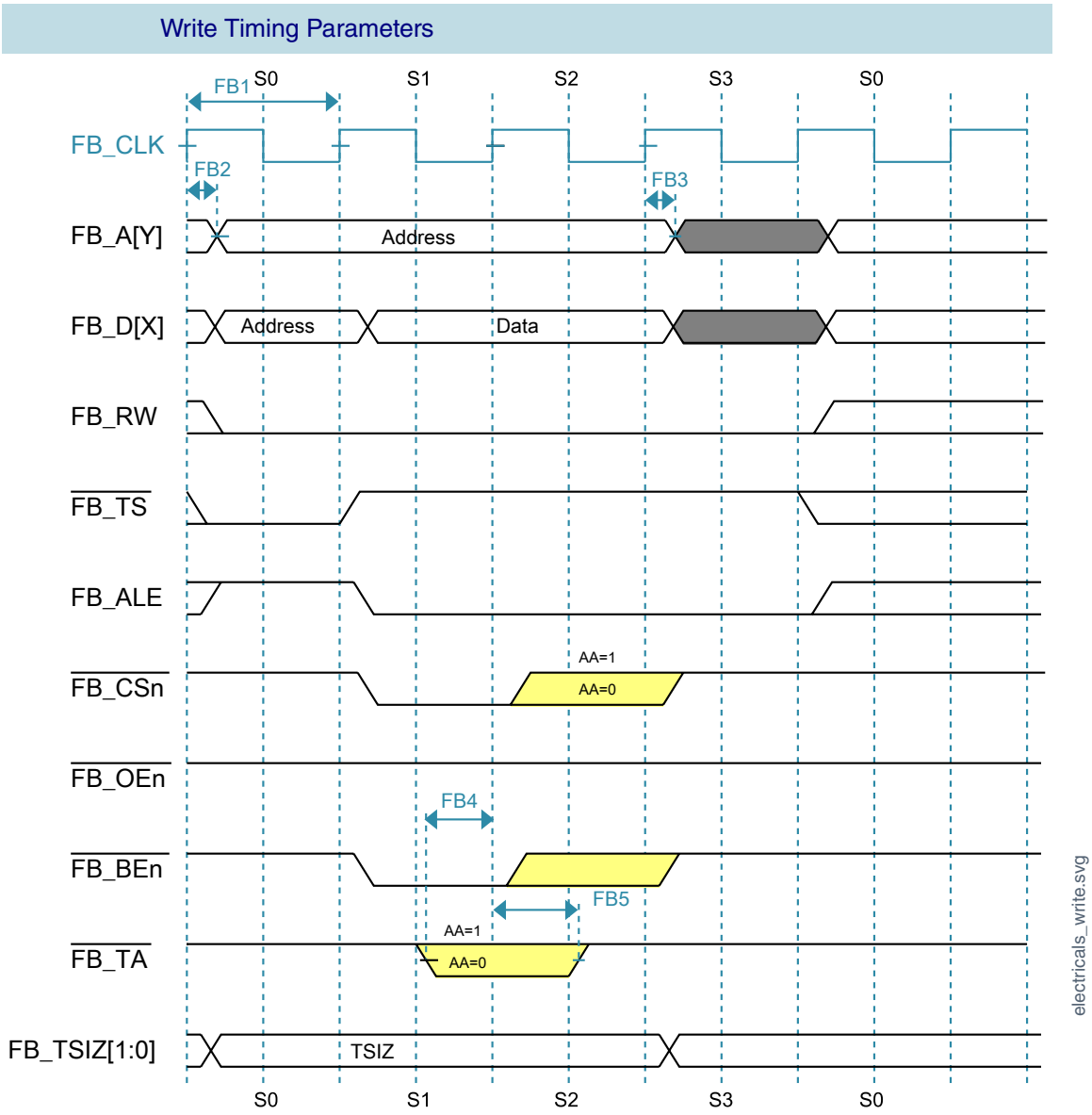


Figure 17. FlexBus write timing diagram

4.4.4.2 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4/4.41/4.5 (Dual Date Rate) timing

4.4.4.2.1 SD/eMMC4.3 (Single Data Rate) AC Timing

The following figure depicts the timing of SD/eMMC4.3

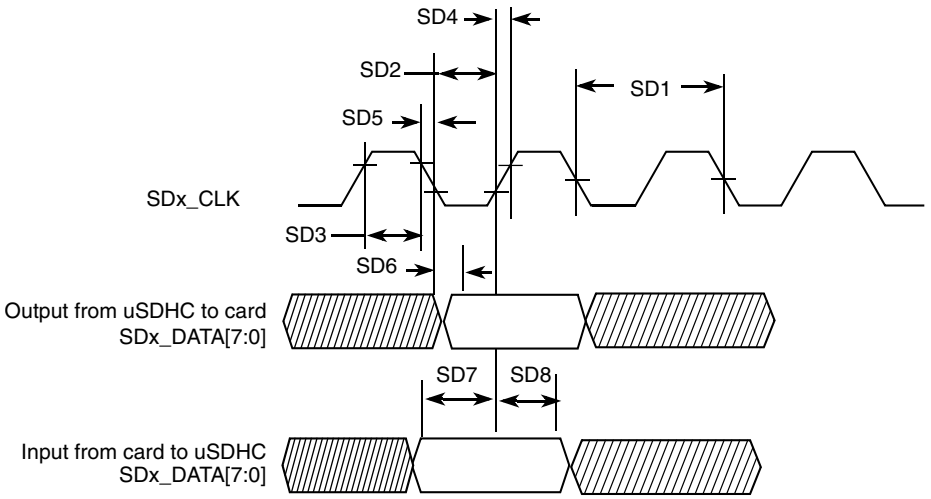


Figure 18. SD/eMMC4.3 timing

The following table lists the SD/eMMC4.3 timing characteristics.

Table 87. SD/eMMC4.3 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	24/48	MHz
	Clock Frequency (MMC Full Speed/ High Speed)	f_{PP}[3]	0	16/48	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1. In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2. In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–24 MHz. In high-speed mode, clock frequency can be any value between 0–48 MHz.
3. In normal (full) speed mode for MMC card, clock frequency can be any value between 0–16 MHz. In high-speed mode, clock frequency can be any value between 0–48 MHz.
4. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.4.4.2.2 eMMC4.4/4.41 (Dual Data Rate) AC Timing

The following figure depicts the timing of eMMC4.4/4.41.

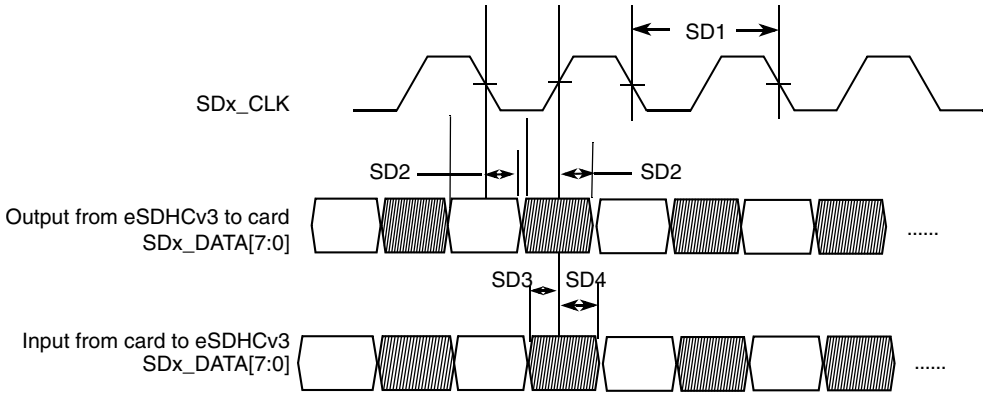


Figure 19. eMMC4.4/4.41 timing

The following table lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

Table 88. eMMC4.4/4.41 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	2.6	—	ns
SD4	uSDHC Input Hold Time	t_{LH}	1.5	—	ns

4.4.4.3 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

4.4.4.3.1 Flash timing specifications — commands

Table 89. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk256k}$	256 KB secondary program flash	—	—	2	ms	
$t_{rd1blk512k}$	512 KB primary program flash	—	—	2	ms	
	Read 1s Section execution time					
$t_{rd1sec2k}$	2 KB flash	—	—	90	µs	1
$t_{rd1sec4k}$	4 KB flash	—	—	100	µs	1
t_{pgmchk}	Program Check execution time	—	—	95	µs	1
t_{pgm8}	Program Phrase execution time	—	110	225	µs	
	Erase Flash Block execution time					2
$t_{ersblk256k}$	256 KB secondary program flash	—	220	2500	ms	
$t_{ersblk512k}$	512 KB primary program flash	—	435	5000	ms	
t_{ersscr}	Erase Flash Sector execution time	—	15	150	ms	2
$t_{pgmsec1k}$	Program Section execution time (1KB flash)	—	8	—	ms	
	Generate CRC execution time (CRCRDY=0)					
t_{crc4}	4 sectors	—	375	425	µs	
t_{crc32}	32 sectors	—	3	3.5	ms	
t_{crc128}	128 sectors	—	12	14	ms	
	Generate CRC execution time (CRCRDY=1)					
t_{crcr4}	4 sectors	—	860	985	µs	
t_{crcr32}	32 sectors	—	7	8	ms	
$t_{crcr128}$	128 sectors	—	28	32	ms	
$t_{rd1allx}$	Read 1s All Blocks execution time	—	—	6	ms	
$t_{rdindex}$	Read Index execution time	—	—	35	µs	1
$t_{pgmindex}$	Program Index execution time	—	110	—	µs	
t_{ersall}	Erase All Blocks execution time	—	1100	13000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	40	µs	1
	Swap Control execution time					
$t_{swapx01}$	control code 0x01	—	350	—	µs	
$t_{swapx02}$	control code 0x02	—	125	250	µs	
$t_{swapx04}$	control code 0x04	—	150	275	µs	
$t_{swapx08}$	control code 0x08	—	—	40	µs	1
$t_{swapx10}$	control code 0x10	—	125	250	µs	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	1100	13000	ms	2

Table continues on the next page...

Table 89. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Set RAM Function execution time					
$t_{setramcc}$	Control Code 0xCC	—	130	—	µs	
$t_{setramff}$	Control Code 0xFF	—	85	—	µs	

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

4.4.4.3.2 Flash high voltage current behaviors

Table 90. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

4.4.4.3.3 Reliability specifications

Table 91. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.

4.4.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

4.4.6 Analog

4.4.6.1 ADC electrical specifications

4.4.6.1.1 ADC operating conditions

Table 92. ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage		1.71	—	3.6	V	2
V_{REFH}	ADC reference voltage high		1.2	—	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage		VREFL	—	Min. of VREFH and VDDIOx[3]	V	4
C_{ADIN}	Input capacitance	• 12-bit mode	—	4	6	pF	
R_{ADIN}	Input series resistance		—	1	5	kΩ	
R_{AS}	Analog source resistance (external)	12-bit mode	—	—	5	kΩ	5
f_{ADCK}	ADC conversion clock frequency	12-bit mode • CFG[PWRSEL]=0b00 • CFG[PWRSEL]=0b01 • CFG[PWRSEL]=0b10 • CFG[PWRSEL]=0b11	 4 4 4 4	 — — — —	 4 8 16 32	MHz	
C_{rate}	ADC conversion rate	12-bit mode, no ADC hardware averaging • CFG[PWRSEL]=0b00 • CFG[PWRSEL]=0b01 • CFG[PWRSEL]=0b10 • CFG[PWRSEL]=0b11	 234.771 234.939 234.853 234.936	 — — — —	 235.546 472.322 248.294 1230.830	ksps	
$t_{ADCSTUP}$	Analog startup time		—	—	4	µs	6

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. V_{DDA} must be equal to the higher of V_{DDIO1} or V_{DDIO2}.
3. VDDIOx is either VDDIO1 or VDDIO2 and is dependent on the IO supply associated with the ADC channel pin. If VREFH is less than VDDIOx, then voltage inputs greater than VREFH but less than VDDIOx are allowed but result in a saturated conversion result.
4. If VREFH is less than VDDA, then voltage inputs greater than VREFH but less than VDDA are allowed but result in a saturated conversion result.

5. This resistance is external to the packaged device. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The $R_{AS} \times C_{AS}$ time constant should be kept to < 1 ns.
6. The startup time is defined as the duration from when (1) CFG[PWREN] is set or (2) when a trigger event initiates command execution until the analog circuits are stable and ready to sample and convert analog input channels. When CFG[PWREN]=0b0, the delay period controlled by CFG[PUDLY] after an initial trigger detect must exceed the analog startup time of $t_{ADCSTUP}$ to guarantee ADC operation.

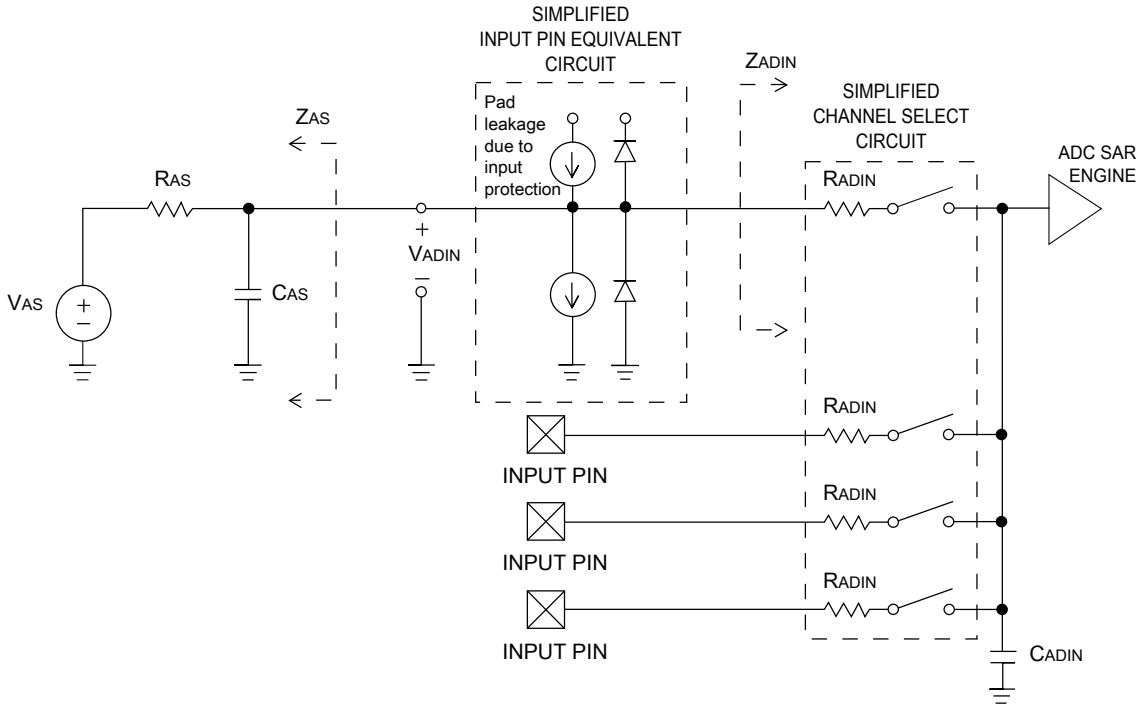


Figure 20. ADC input impedance equivalency diagram

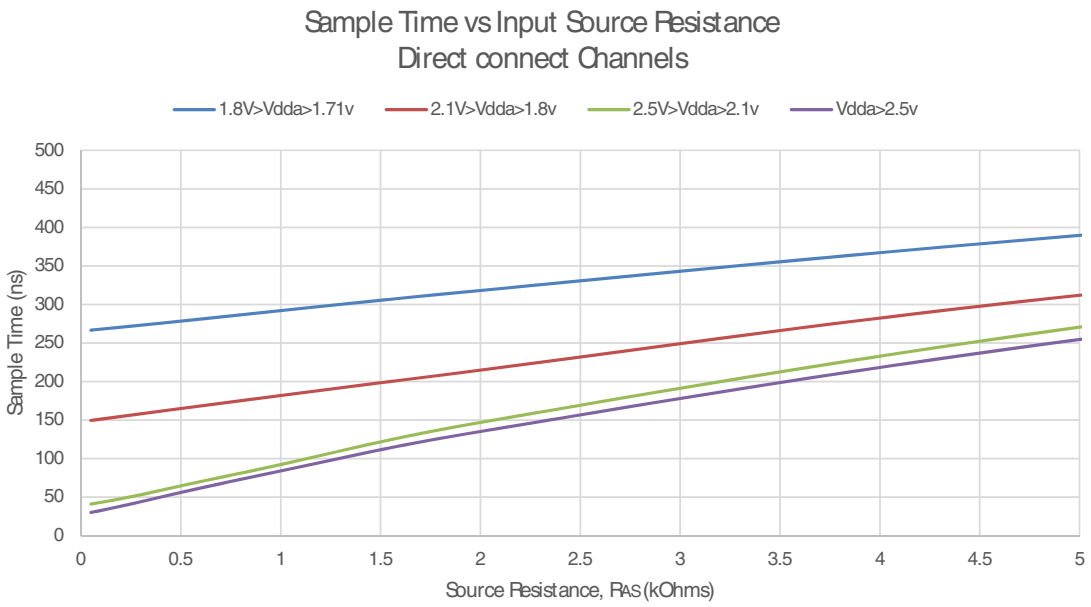


Figure 21. Sample time vs input source resistance direct connect channels

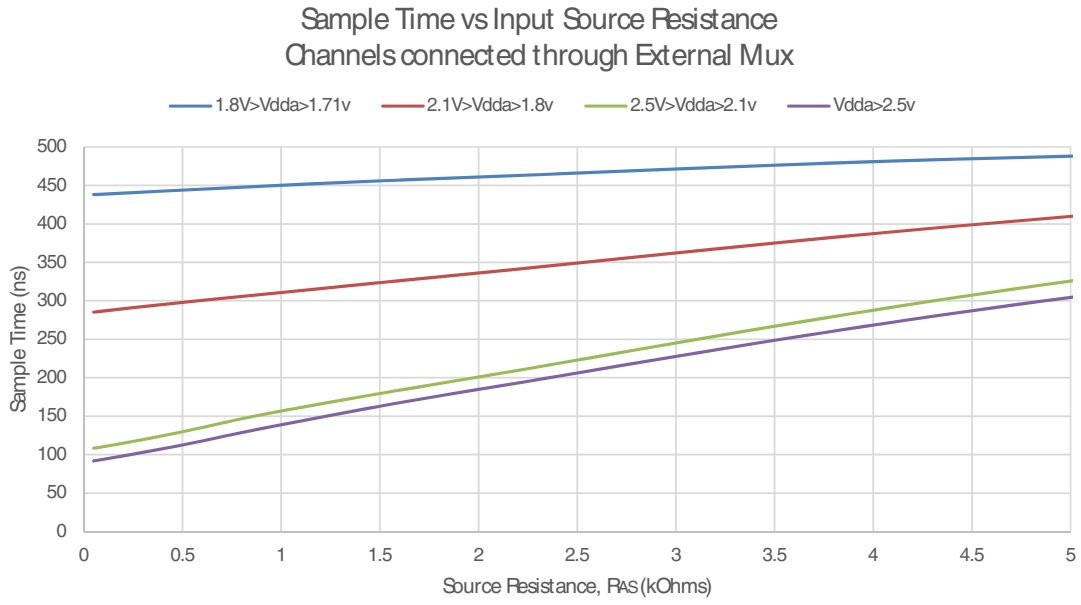


Figure 22. Sample time vs input source resistance channels connected through external mux

NOTE

Direct connect channels are channels that are purely analog channels and do not have any digital options. These include LPADC0_SE15 and LPADC0_SE16. All other channels are MUXed channels.

4.4.6.1.2 ADC electrical characteristics

Table 93. ADC characteristics (V_{REFH} = 3.0 V, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ. [2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current	CFG[PWRSEL]=0b00, f_{ADCK} = 4 MHz	—	25	40	µA	3
		CFG[PWRSEL]=0b01, f_{ADCK} = 12 MHz	—	60	95	µA	
		CFG[PWRSEL]=0b10, f_{ADCK} = 24 MHz	—	120	190	µA	
		CFG[PWRSEL]=0b11, f_{ADCK} = 48 MHz	—	220	380	µA	
I_{DDA_ADC}	Supply current	ADC Idle, analog pre-enabled (CFG[PWREN]=0b1)	—	10	—	µA	
f_{ADACK}	ADC asynchronous clock source		—	2	—	MHz	
Δf_{ADACK_T}	Deviation of ADACK clock due to temperature		—	±7%	—		
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit mode	—	±4	±6.8	LSB[4]	5
DNL	Differential non-linearity	• 12-bit mode	—	±0.7	–1.1 to +1.9	LSB[4]	5
INL	Integral non-linearity	• 12-bit mode	—	±1.0	–2.7 to +1.9	LSB[4]	5
E_{FS}	Full-scale error	• 12-bit mode	—	–4	–5.4	LSB[4]	V_{ADIN} = V_{REFH}[5]
E_Q	Quantization error	• 12-bit mode	—	—	±0.5	LSB[4]	
ENOB	Effective number of bits	12-bit single-ended mode					6
		• Avg = 16	—	10.7	—	bits	
		• Avg = 4	—	10.3	—	bits	
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	7
	Temp sensor slope	Across the full temperature range of the device	1.70	1.78	1.85	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	701	711	721	mV	8

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = 3.0 V
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C unless otherwise stated. Typical values are for reference only and are not tested in production.
3. Shortest sample time (CMDH*a*[STS]=0x0), continuous operation (command execution set for single or multi-command sequential loop).
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

5. ADC conversion clock < 32 MHz, Max hardware averaging (CMDH*a*[AVGS] = 0x7)
6. Input data is 500 Hz sine wave. ADC conversion clock < 32 MHz.
7. I_{In} = leakage current. Refer to pin leakage specification in the packaged device's voltage and current operating ratings.
8. Set CFG[STS]=0b111.

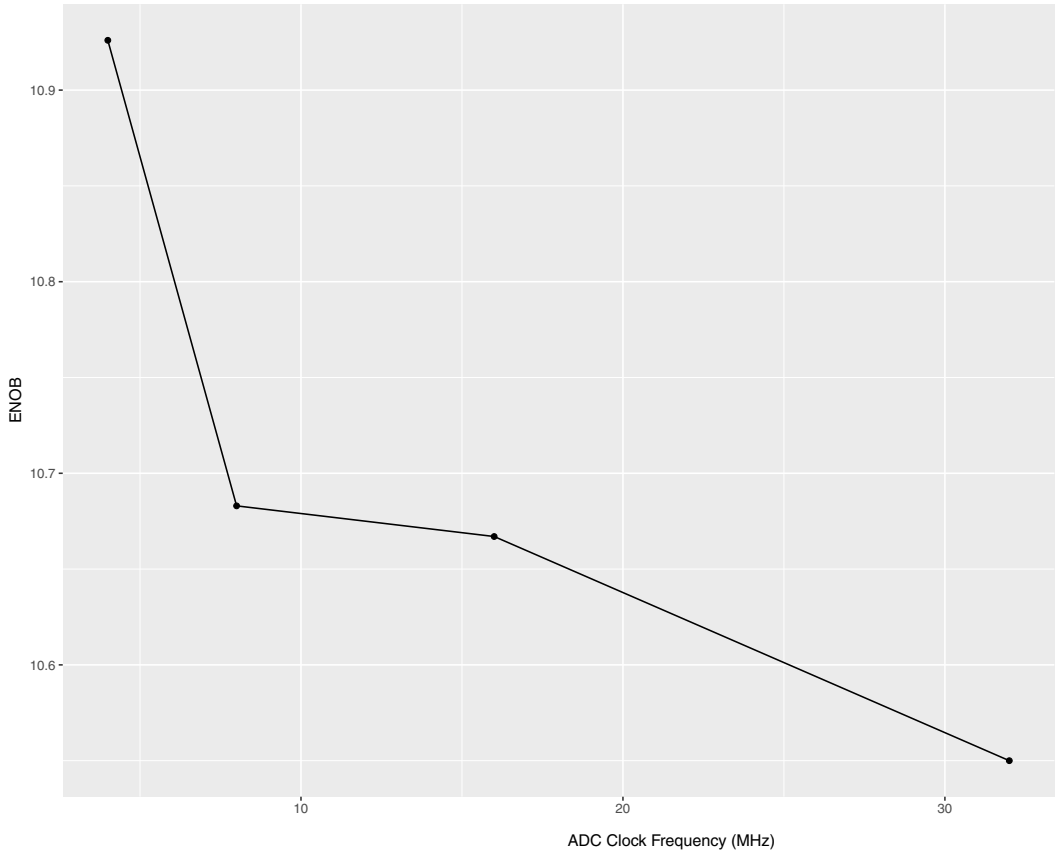


Figure 23. Typical ENOB vs. ADCK for 12-bit single-ended mode

4.4.6.2 Voltage reference electrical specifications

Table 94. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage for 1.2V output	1.71	3.6	V	—
	Supply voltage for 2.1V output	2.4	3.6	V	—
T_A	Temperature	Operating temperature range of the device		°C	—
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 95. VREF full-range operating behaviors

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal VDDA and temperature=25 °C	1.2 V range	1.19	1.195	1.2	V	1
		2.1 V range	2.091	2.1	2.109	V	1
V_{step}	Voltage reference trim step for 1.2 V output		—	0.5	—	mV	1
	Voltage reference trim step for 2.1 V output		—	1.0	—	mV	1
I_{bg}	Bandgap only current		—	60	80	µA	1
I_{lp}	Low-power buffer current		—	180	360	µA	1
I_{hp}	High-power buffer current		—	480	960	µA	1
ΔV_{LOAD}	Load regulation — current is ± 1.0 mA		—	±0.2	—	mV	1, 2
T_{stup}	Buffer startup time		—	—	100	µs	—
V_{vdrift}	Voltage drift for 1.2 V output (Vmax -Vmin across the full voltage range)		—	0.5	2	mV	1
	Voltage drift for 2.1 V output (Vmax -Vmin across the full voltage range)		—	0.9	3.5	mV	
V_{tdrift}	Temperature drift for 1.2 V output (Vmax -Vmin across the full temperature range)		—	2	15	mV	3
	Temperature drift for 2.1 V output (Vmax -Vmin across the full temperature range)		—	3.5	27	mV	

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register for V_{out} selection of 1.2 V or 2.1 V.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load
3. To get best performance of VREF temperature drift, VREF_SC[ICOMPEN] must be set.

4.4.6.3 CMP and 6-bit DAC electrical specifications

Table 96. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}[1]	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, high-speed mode (EN=1, HPMD=1)	—	—	180	µA
I_{DDLS}	Supply current, normal mode (EN=1, HPMD=0, NPMD=0)	—	—	20	µA
I_{DDNS}	Supply current, nano mode (EN=1, HPMD=0, NPMD=1)	—	—	0.390	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[2]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
		—	20	—	mV

Table continues on the next page...

Table 96. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	• CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[3]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[4]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. For LPCMP0 $V_{DD} = V_{DDIO1}$; for LPCMP1, $V_{DD} = V_{DDIO2}$.
2. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
3. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
4. 1 LSB = $V_{reference}/64$

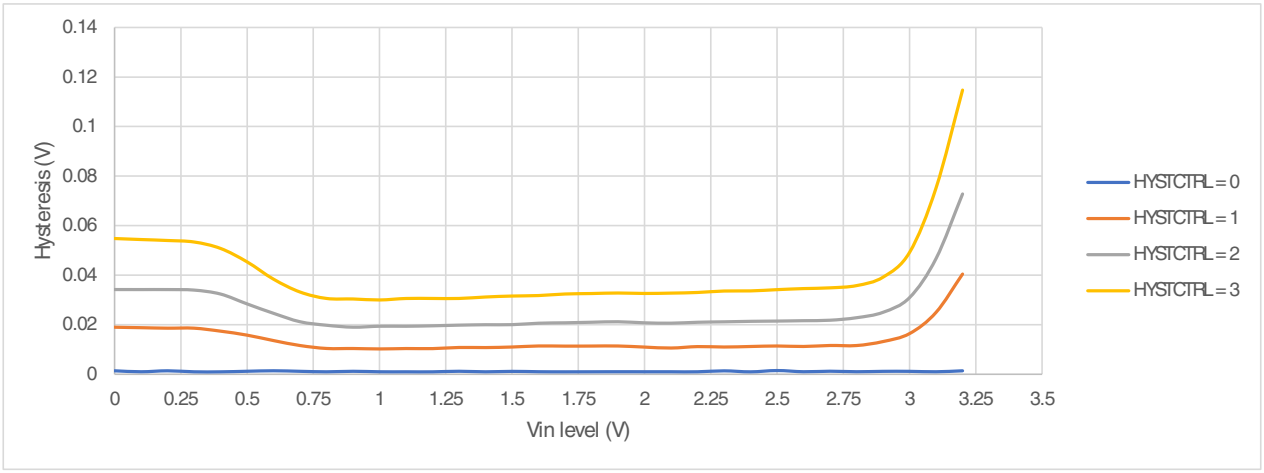


Figure 24. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 1)

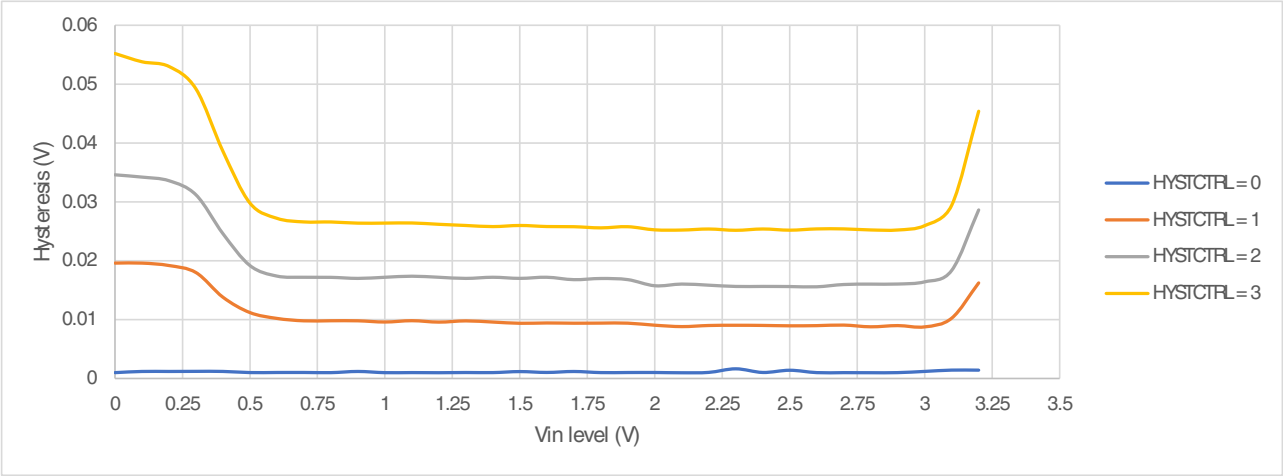


Figure 25. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 0)

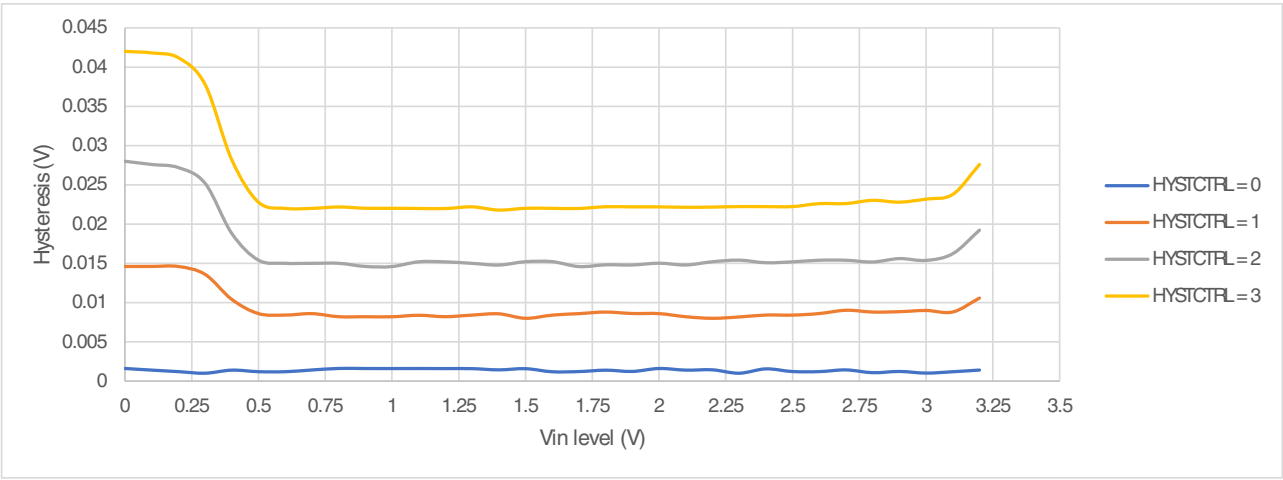


Figure 26. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 1)

4.4.6.4 12-bit DAC electrical characteristics

4.4.6.4.1 12-bit DAC operating requirements

Table 97. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REF_OUT}.

2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

4.4.6.4.2 12-bit DAC operating behaviors

Table 98. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	250	µA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	900	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	
	• High power (SP_{HP})	1.2	1.7	—		
	• Low power (SP_{LP})	0.05	0.12	—		
BW	3dB bandwidth				kHz	
	• High power (SP_{HP})	550	—	—		
	• Low power (SP_{LP})	40	—	—		

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV

6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

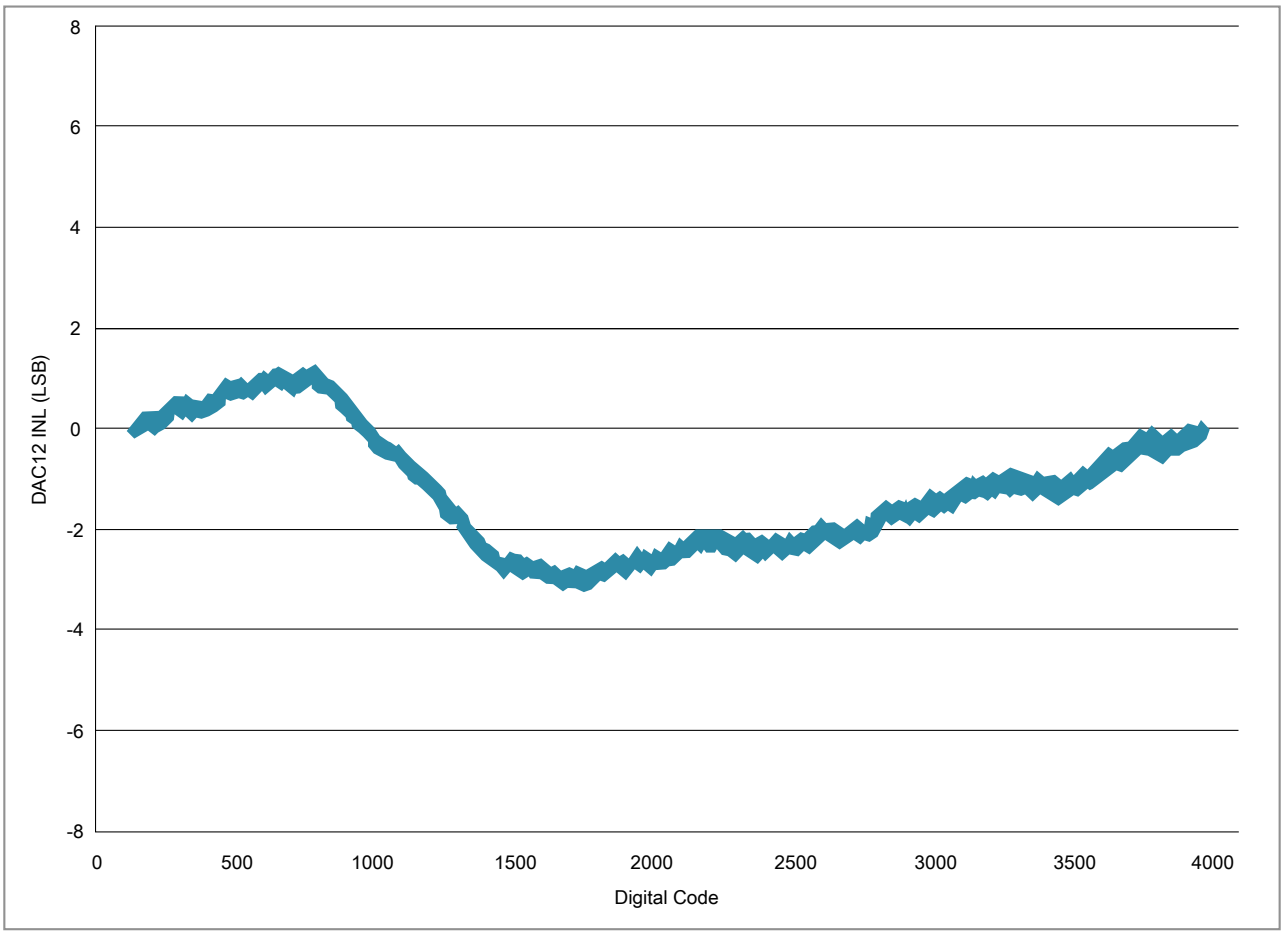


Figure 27. Typical INL error vs. digital code

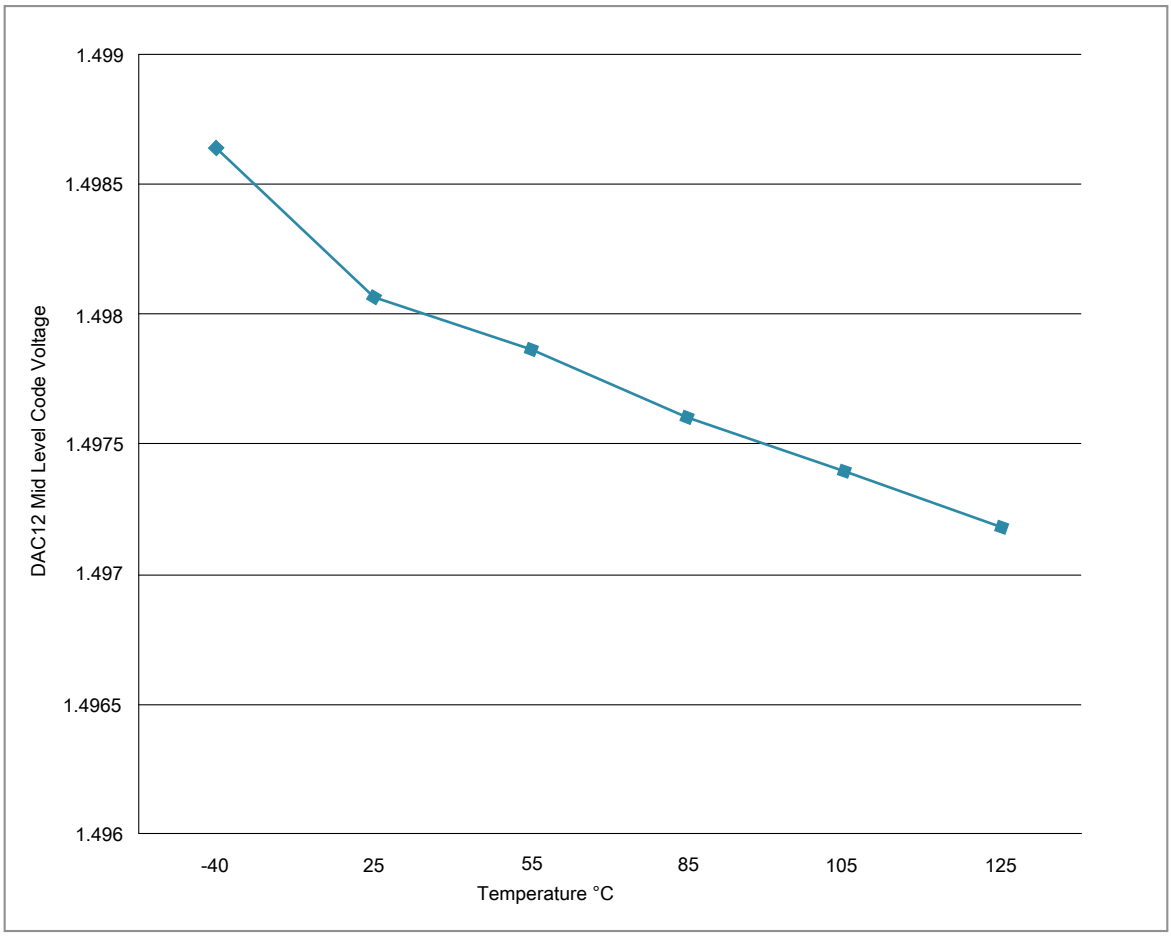


Figure 28. Offset at half scale vs. temperature

4.4.7 Timers

See General switching specifications.

4.4.8 Communication interfaces

4.4.8.1 EMV SIM specifications

Each EMV SIM module interface consists of a total of five pins.

The interface is designed to be used with synchronous Smart cards, meaning the EMV SIM module provides the clock used by the Smart card. The clock frequency is typically 372 times the Tx/Rx data rate; however, the EMV SIM module can also work with CLK frequencies of 16 times the Tx/Rx data rate.

There is no timing relationship between the clock and the data. The clock that the EMV SIM module provides to the Smart card is used by the Smart card to recover the clock from the data in the same manner as standard UART data exchanges. All five signals of the EMV SIM module are asynchronous with each other.

The smart card is initiated by the interface device; the Smart card responds with Answer to Reset. Although the EMV SIM interface has no defined requirements, the ISO/IEC 7816 defines reset and power-down sequences (for detailed information see ISO/IEC 7816).

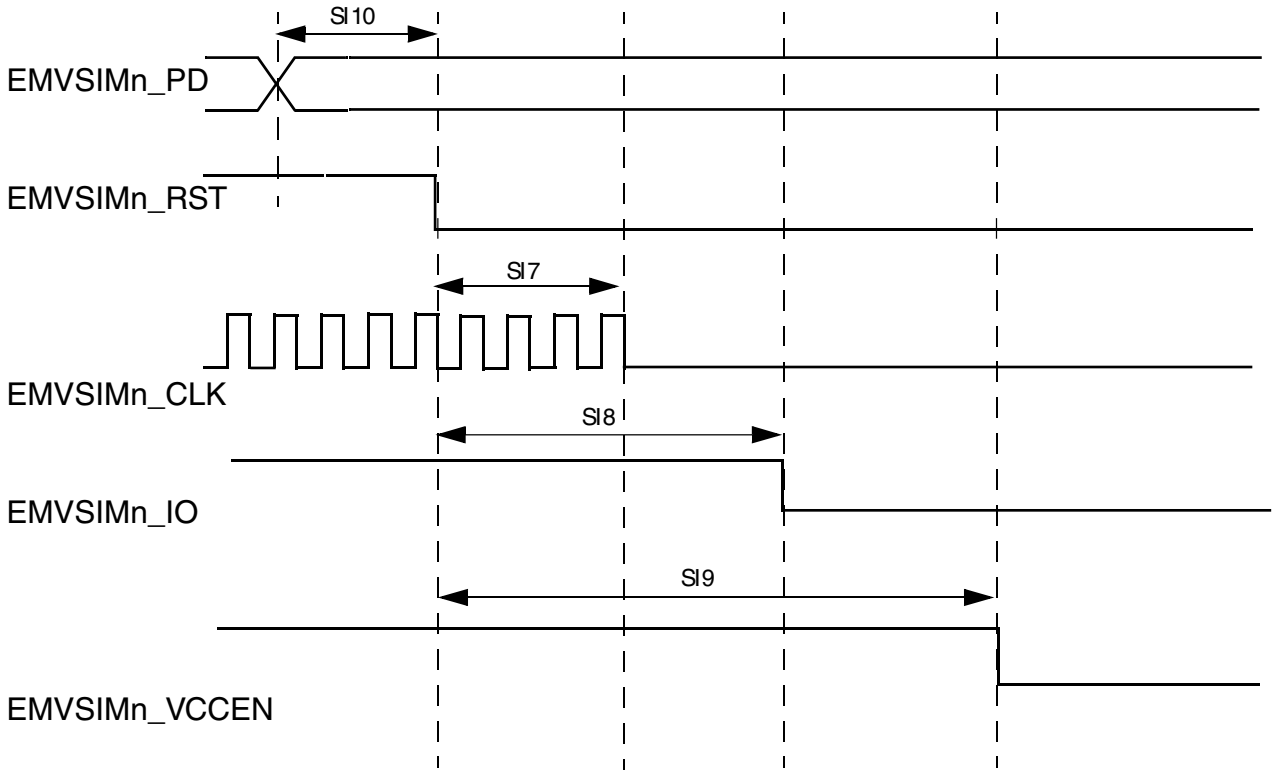


Figure 29. EMV SIM Clock Timing Diagram

The following table defines the general timing requirements for the EMV SIM interface.

Table 99. Timing Specifications, High Drive Strength

ID	Parameter	Symbol	Min	Max	Unit
SI 1	EMV SIM clock frequency (EMVSIMn_CLK)[1]	S_{freq}	1	5	MHz
SI 2	EMV SIM clock rise time (EMVSIMn_CLK)[2]	S_{rise}	—	0.08 × (1/Sfreq)	ns
SI 3	EMV SIM clock fall time (EMVSIMn_CLK)[2]	S_{fall}	—	0.08 × (1/Sfreq)	ns

Table continues on the next page...

Table 99. Timing Specifications, High Drive Strength (continued)

ID	Parameter	Symbol	Min	Max	Unit
SI 4	EMV SIM input transition time (EMVSIMn_IO, EMVSIMn_PD)	S_{tran}	20	25	ns
Si 5	EMV SIM I/O rise time / fall time (EMVSIMn_IO)[3]	Tr/Tf	—	0.8	µs
Si 6	EMV SIM RST rise time / fall time (EMVSIMn_RST)[4]	Tr/Tf	—	0.8	µs

1. 50% duty cycle clock,
2. With C = 50 pF
3. With Cin = 30 pF, Cout = 30 pF,
4. With Cin = 30 pF,

4.4.8.1.1 EMV SIM Reset Sequences

Smart cards may have internal reset, or active low reset. The following subset describes the reset sequences in these two cases.

4.4.8.1.1.1 Smart Cards with Internal Reset

Following figure shows the reset sequence for Smart cards with internal reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on EMVSIMn_CLK (time T0)
- After 200 clock cycles, EMVSIMn_IO must be asserted.
- The card must send a response on EMVSIMn_IO acknowledging the reset between 400–40000 clock cycles after T0.

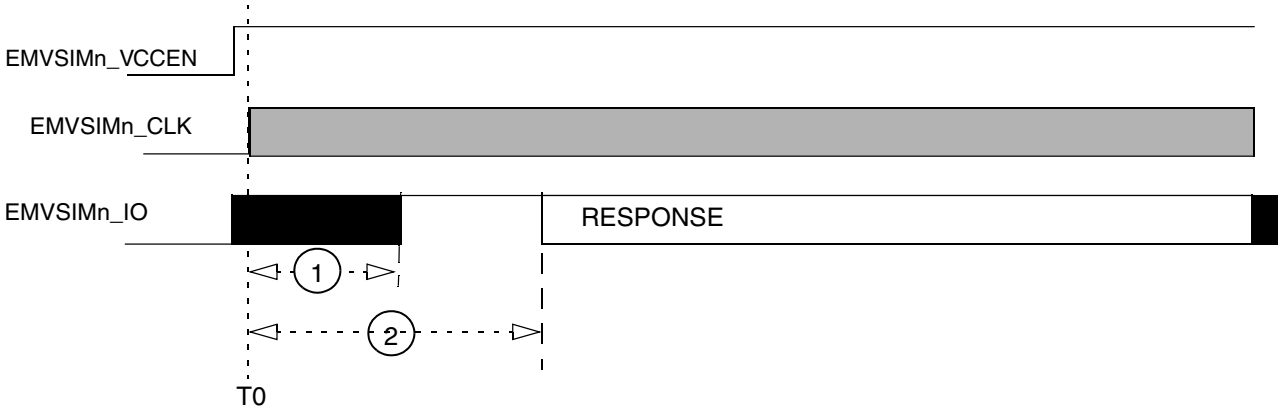


Figure 30. Internal Reset Card Reset Sequence

The following table defines the general timing requirements for the SIM interface.

Table 100. Timing Specifications, Internal Reset Card Reset Sequence

Ref	Min	Max	Units
1	—	200	EMVSIMx_CLK clock cycles
2	400	40,000	EMVSIMx_CLK clock cycles

4.4.8.1.1.2 Smart Cards with Active Low Reset

Following figure shows the reset sequence for Smart cards with active low reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on EMVSIMn_CLK (time T0)
- After 200 clock cycles, EMVSIMn_IO must be asserted.
- EMVSIMn_RST must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
- EMVSIMn_RST is asserted (at time T1)
- EMVSIMn_RST must remain asserted for at least 40,000 clock cycles after T1, and a response must be received on EMVSIMn_IO between 400 and 40,000 clock cycles after T1.

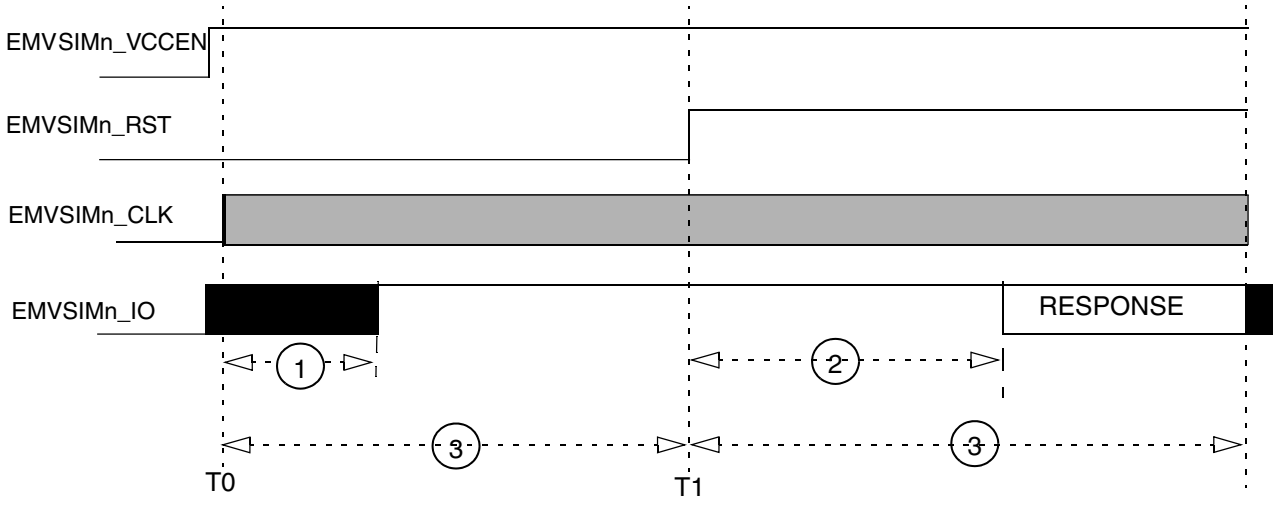


Figure 31. Active-Low-Reset Smart Card Reset Sequence

The following table defines the general timing requirements for the EMVSIM interface..

Table 101. Timing Specifications, Internal Reset Card Reset Sequence

Ref No	Min	Max	Units
1	—	200	EMVSIMx_CLK clock cycles
2	400	40,000	EMVSIMx_CLK clock cycles
3	40,000	—	EMVSIMx_CLK clock cycles

4.4.8.1.2 EMVSIM Power-Down Sequence

Following figure shows the EMV SIM interface power-down AC timing diagram.Table 102 table shows the timing requirements for parameters (SI7–SI10) shown in the figure. The power-down sequence for the EMV SIM interface is as follows:

- EMVSIMn_SIMPD port detects the removal of the Smart Card
- EMVSIMn_RST is negated
- EMVSIMn_CLK is negated
- EMVSIM_IO is negated
- EMVSIMx_VCCENy is negated

Each of the above steps requires one OSC32KCLK period (usually 32 kHz, also known as rtcclk in below figure). Power-down may be initiated by a Smart card removal detection; or it may be launched by the processor.

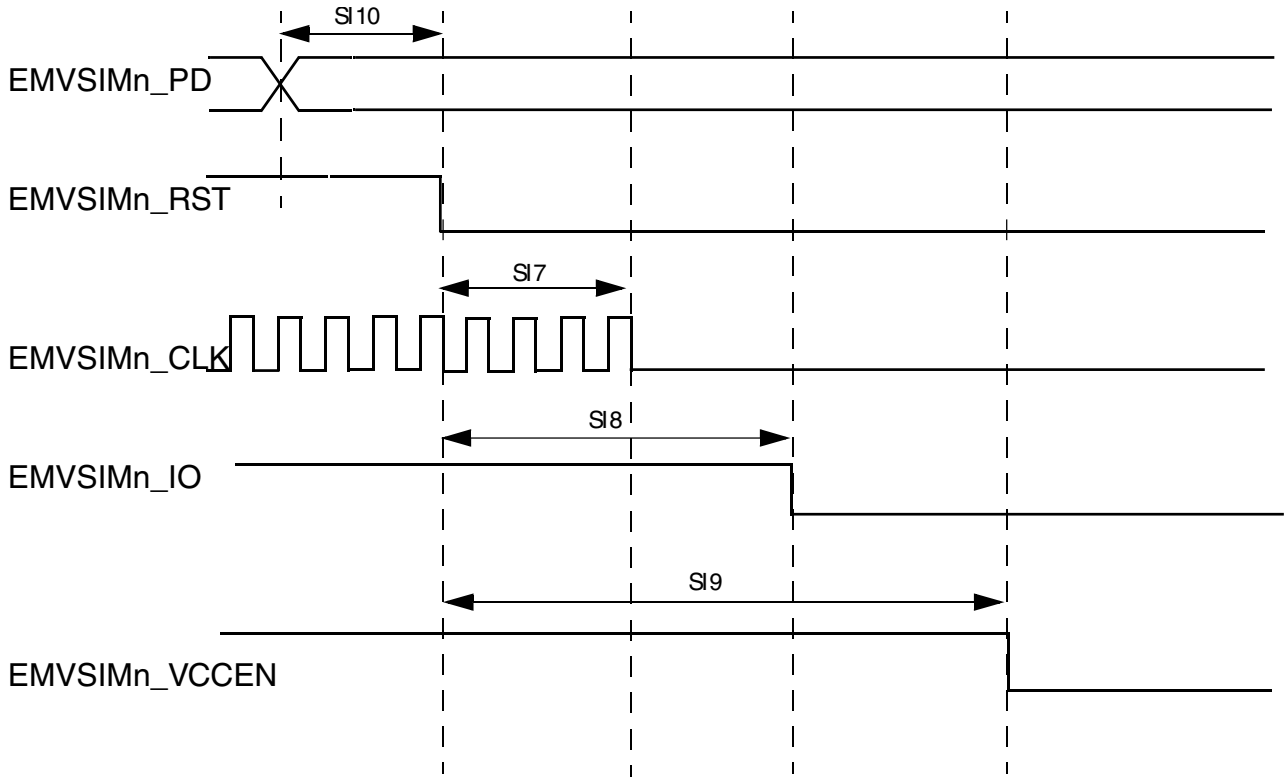


Figure 32. Smart Card Interface Power Down AC Timing

Table 102. Timing Requirements for Power-down Sequence

Ref No	Parameter	Symbol	Min	Max	Units
SI7	EMVSIM reset to SIM clock stop	$S_{rst2clk}$	0.9 × 1/ Frtcclk[1]	1.1 × 1/Frtcclk	µs
SI8	EMVSIM reset to SIM Tx data low	$S_{rst2dat}$	1.8 × 1/Frtcclk	2.2 × 1/Frtcclk	µs
SI9	EMVSIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7 × 1/Frtcclk	3.3 × 1/Frtcclk	µs
SI10	EMVSIM presence detect to SIM reset low	S_{pd2rst}	0.9 × 1/Frtcclk	1.1 × 1/Frtcclk	µs

1. Frtcclk is OSC32KCLK, and this clock must be enabled during the power down sequence.

NOTE

Same timing is also followed when auto power down is initiated. See Reference Manual for reference.

4.4.8.2 USB electrical specifications

The USB electricals for the USB module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit **usb.org**.

NOTE

The IRC48M meets the USB jitter specifications for certification in Device mode when the USB clock recovery mode is enabled. It does not meet the USB jitter specifications for certification in Host mode operation.

This device does not have the USB_CLKIN signal available and therefore cannot support Host mode operation.

4.4.8.3 USB VREG electrical specifications

Table 103. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	— —	650 —	— 4	nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

4.4.8.4 LPSPI switching specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

NOTE

- Slew rate disabled pads are those pins with PORTx_PCRn[SRE] bit cleared. Slew rate enabled pads are those pins with PORTx_PCRn[SRE] bit set.
- To achieve high bit rate, it is recommended to use fast pins (PTB[2,0], PTD[7:2], PTE[12,9:8,5:1]) and/or high drive pins (PTC[12:7], PTD[11:8], PTE[11:10]).

Table 104. LPSPI master mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} is the LPSPI peripheral functional clock.
2. $t_{periph} = 1/f_{periph}$

Table 105. LPSPI master mode timing on slew rate enabled pads

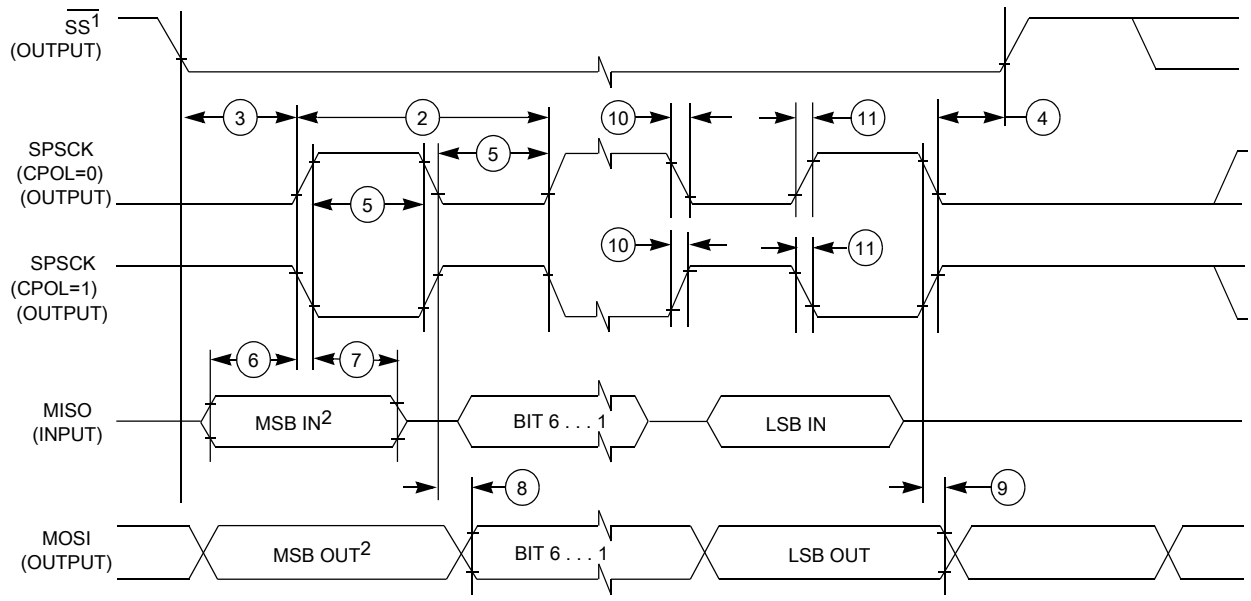
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2

Table continues on the next page...

Table 105. LPSPI master mode timing on slew rate enabled pads (continued)

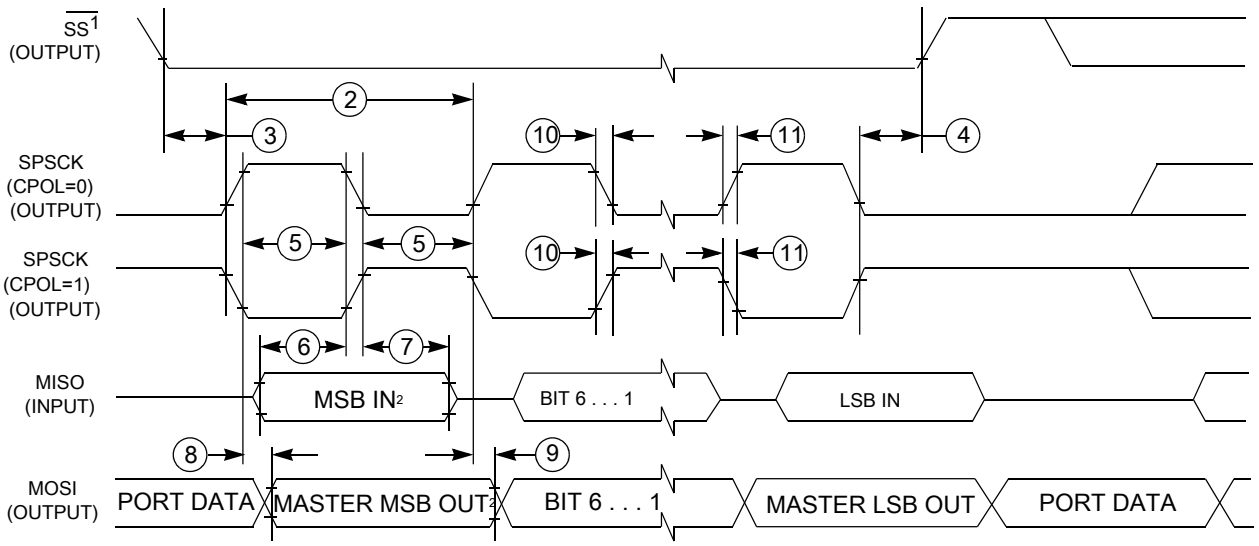
Num.	Symbol	Description	Min.	Max.	Unit	Note
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. f_{periph} is the LPSPI peripheral functional clock
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 33. LPSPI master mode timing (CPHA = 0)



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 34. LPSPI master mode timing (CPHA = 1)

Table 106. LPSPI slave mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} is the LPSPI peripheral functional clock
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

Table 107. LPSPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. f_{periph} is the LPSPI peripheral functional clock
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

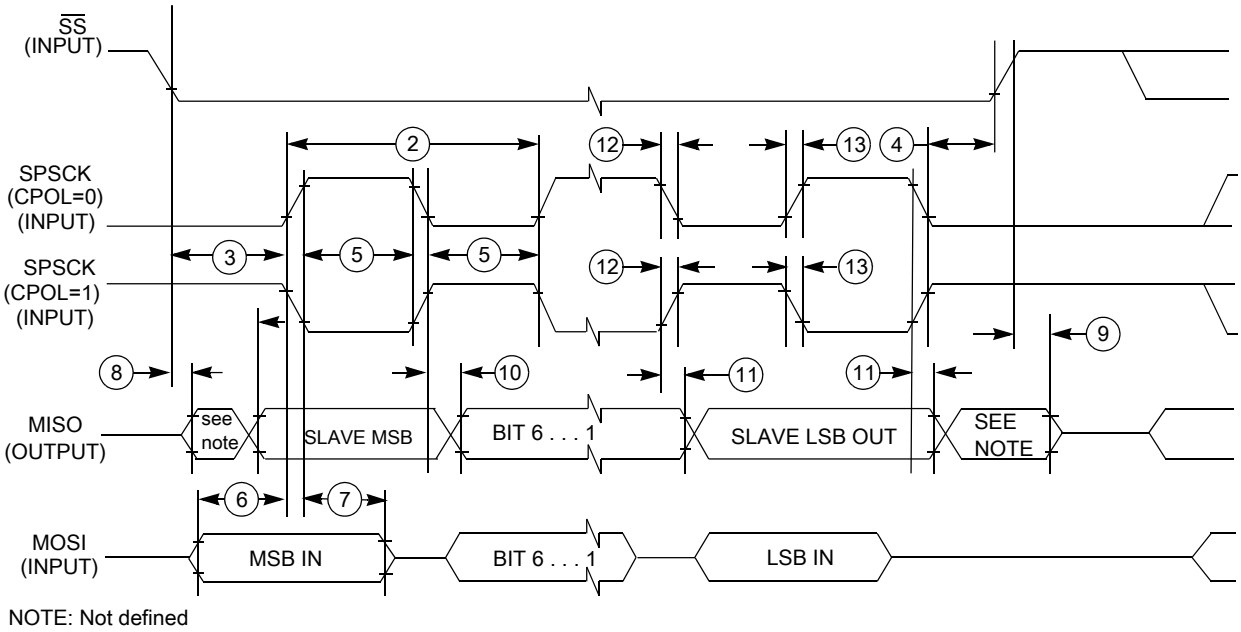


Figure 35. LPSPI slave mode timing (CPHA = 0)

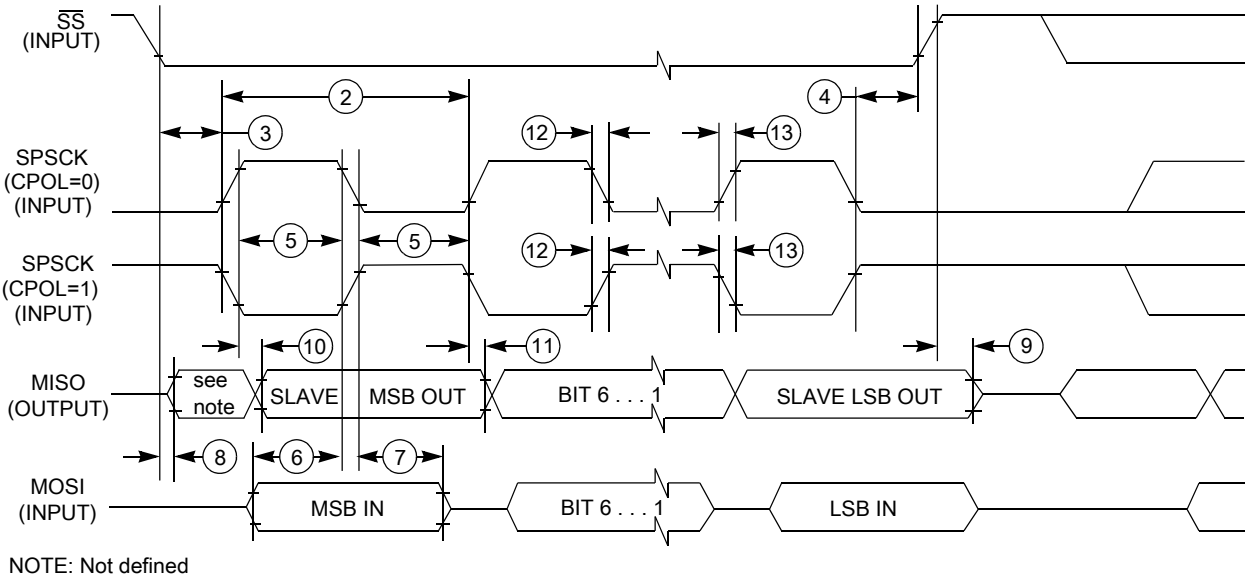


Figure 36. LPSPI slave mode timing (CPHA = 1)

4.4.8.5 LPI2C

NOTE

The LPI2C async function clock must not be faster than 24 MHz.

Table 108. LPI2C specifications

Symbol	Description		Min.	Max.	Unit	Notes
f_{SCL}	SCL clock frequency	Standard mode (Sm)	0	100	kHz	1
		Fast mode (Fm)	0	400		1, 2
		Fast mode Plus (Fm+)	0	1000		1, 3
		Ultra Fast mode (UFm)	0	5000		1, 4
		High speed mode (Hs-mode)	0	3400		1, 5

1. See General switching specifications, measured at room temperature.
2. Measured with the maximum bus loading of 400pF at 3.3V VDD with pull-up Rp = 580Ω on normal drive pins or 350Ω on high drive pins, and at 1.8V VDD with Rp = 880Ω. For all other cases, select appropriate Rp per I2C Bus Specification and the pin drive capability.
3. Fm+ is only supported on high drive pin with high drive enabled. It is measured with the maximum bus loading of 400pF at 3.3V VDD with Rp = 350Ω. For all other cases, select appropriate Rp per I2C Bus Specification and the pin drive capability.
4. UFm is only supported on high drive pin with high drive enabled and push-pull output only mode. It is measured at 3.3V VDD with the maximum bus loading of 400pF. For 1.8V VDD, the maximum speed is 4Mbps.
5. Hs-mode is only supported in slave mode and on the high drive pins with high drive enabled.

4.4.8.6 LPUART

See General switching specifications.

4.4.8.7 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

4.4.8.7.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 109. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15.5	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	19	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	26	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

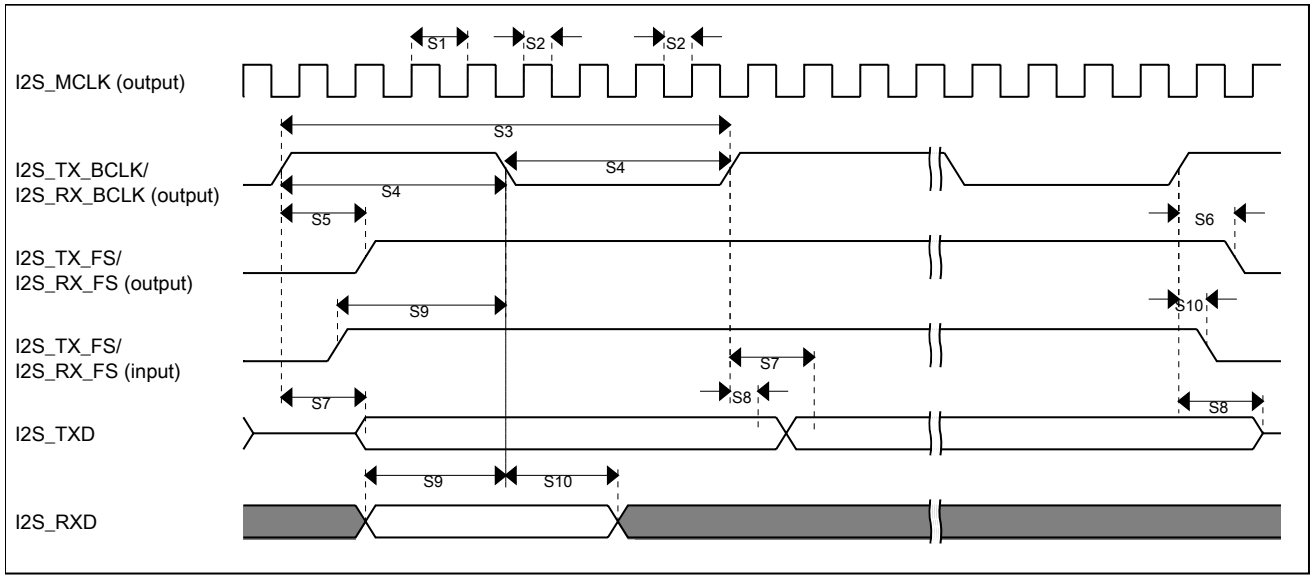


Figure 37. I2S/SAI timing — master modes

Table 110. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	33	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	28	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

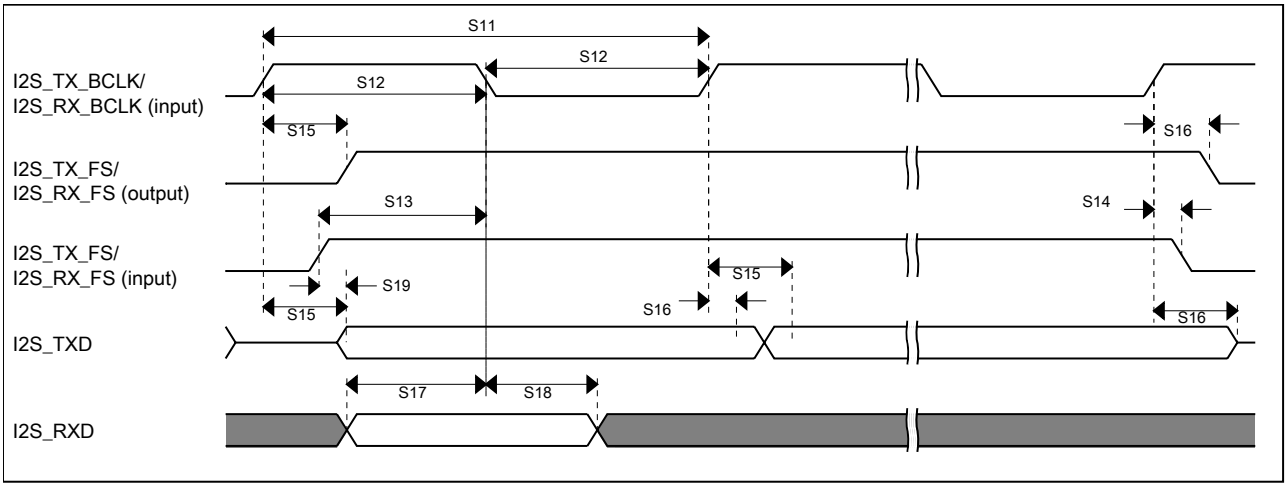


Figure 38. I2S/SAI timing — slave modes

4.4.8.7.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 111. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid		—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid		—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK		—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

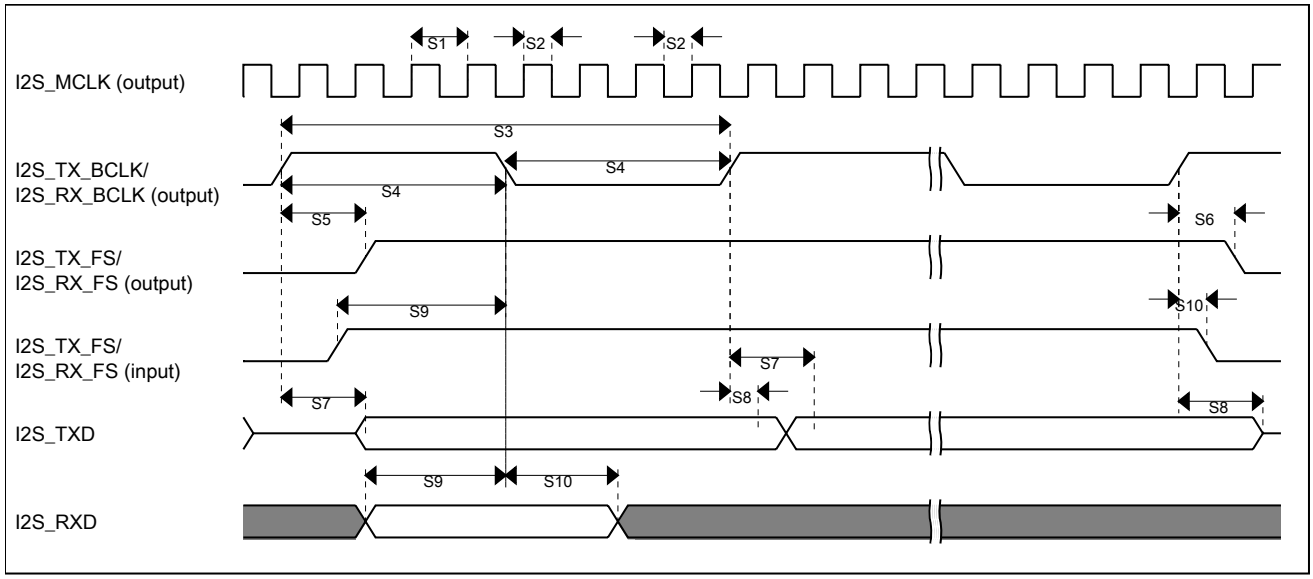


Figure 39. I2S/SAI timing — master modes

Table 112. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK		—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—		ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK		—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

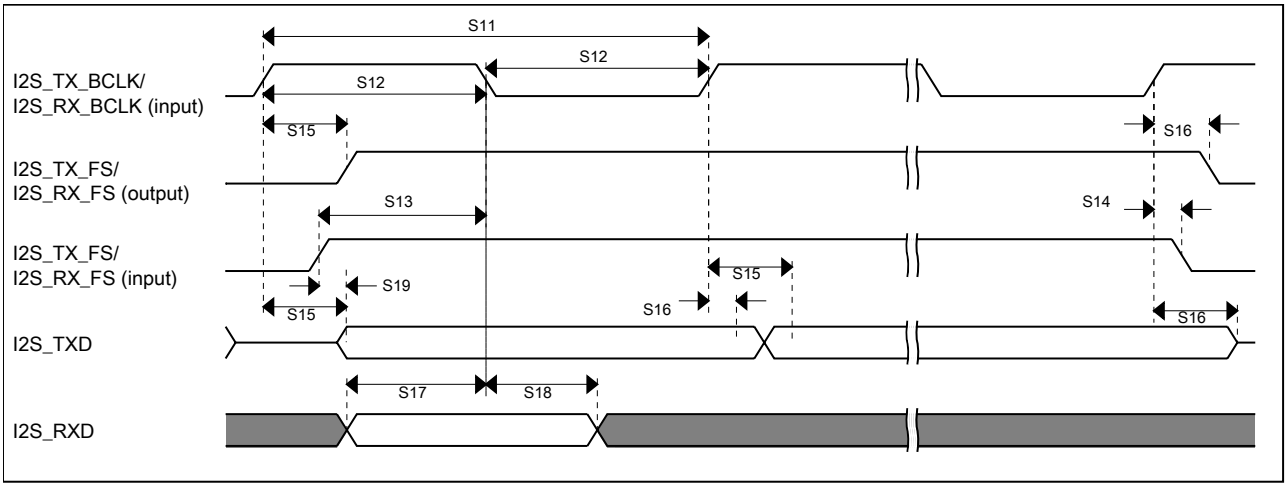


Figure 40. I2S/SAI timing — slave modes

4.4.9 DC-DC Converter Recommended Electrical Characteristics

Table 113. DC-DC Converter Recommended operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit
DCDC Supply Voltage[1, 2, 3]	VDD_{DCDC_IN}	2.1	—	3.6	V
External Inductor	L_DCDC		10		µH
Inductor Resistance in Buck Mode	ESR	—	0.2	0.5	Ohms

1. The DC-DC converter generates 1.8 V at VOUT_AUX and 1.225 V at VOUT_CORE pins. VOUT_AUX can be used to power the VDDIOx and VDDA supplies.
2. The DCDC converter generates 1.225 V at VOUT_CORE. This can be used to power the VDD_CORE supplies. This supply must not be used to power any additional circuitry.
3. In Buck mode, DC-DC converter needs 2.1 V min to start, the supply can drop to 1.8 V (or VOUT_AUX target value + 50 mV; whichever is higher) after DC-DC converter settles.

Table 114. DC-DC Converter Specifications

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
DC-DC Converter Output Power	Total power output of VOUT_AUX and VOUT_CORE	Pdcdc_out	—	—	125	mW
DC-DC Converter input voltage	—	VDCDC_IN	2.1	—	3.6	Vdc
DC-DC Converter output Voltage	—	VOUT_AUX	1.800	—	2.075	Vdc
	RUN mode	VOUT_CORE	1.225	1.225	1.325	Vdc
	HSRUN mode	VOUT_CORE	1.400	1.400	1.450	Vdc
DCDC Turn on Time	—	T_{DCDC_ON}	—	5[1]	—	ms

Table continues on the next page...

Table 114. DC-DC Converter Specifications (continued)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
VOUT_AUX Output Current	—	IOUT_AUX	—	—	100	mA
VOUT_CORE Output Current	—	IOUT_CORE	—	—	100	mA
Switching frequency	—	DCDC_FREQ	—	2	—	MHz
DCDC Conversion Efficiency	—	DCDC_EFF_buck	—	90%	—	
DCDC Settling Time for increasing voltage		$T_{DCDC\_SETTLE\_buck}$	—	260	—	ms/V
DCDC Settling Time for decreasing voltage		$T_{DCDC\_SETTLE\_buck}$	—	38	—	ms/V

1. Based on LDO is on and output at 1.8 V and 1.2 V. DCDC set to 1.8 V and 1.235 V

5 Design considerations

5.1 Hardware design considerations

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

5.1.1 Printed circuit board recommendations

- Place connectors or cables on one edge of the board and do not place digital circuits between connectors.
- Drivers and filters for I/O functions must be placed as close to the connectors as possible. Connect TVS devices at the connector to a good ground. Connect filter capacitors at the connector to a good ground.
- Physically isolate analog circuits from digital circuits if possible.
- Place input filter capacitors as close to the MCU as possible.
- For best EMC performance, route signals as transmission lines; use a ground plane directly under LQFP packages; and solder the exposed pad (EP) to ground directly under QFN packages.

5.1.2 Power delivery system

Consider the following items in the power delivery system:

- Use a plane for ground.

- Use a plane for MCU VDDIOx supply if possible.
- Always route ground first, as a plane or continuous surface, and never as sequential segments.
- Route power next, as a plane or traces that are parallel to ground traces.
- Place bulk capacitance, 10 µF or more, at the entrance of the power plane.
- Place bypass capacitors for MCU power domain as close as possible to each VDDIOx/VSS pair, including VDDA/VSSA and VREFH/VREFL.
- The minimum bypass requirement is to place 0.1 µF capacitors positioned as near as possible to the package supply pins.
- It is recommended to include a filter circuit with one bulk capacitor (no less than 2.2 µF) and one 0.1 µF capacitor at the VREGIN and VOUT33 pins to improve USB performance.
- Take special care to minimize noise levels on the VREFH/VREFL inputs. An option is to use the internal reference voltage (output 1.2 V/2.1 V typically) as the ADC reference.
- VDDIO2 is dedicated to powering PORTE.
- VDDA must be higher or equal to the greater of VDDIO1 and VDDIO2.

5.1.3 Analog design

Each ADC input must have an RC filter as shown in the following figure. The maximum value of R must be RAS max if fast sampling and high resolution are required. The value of C must be chosen to ensure that the RC time constant is very small compared to the sample period.

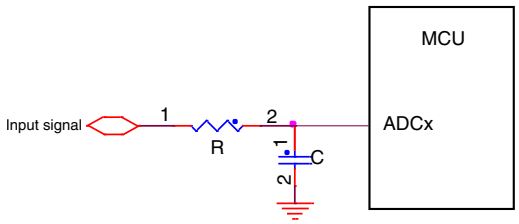


Figure 41. RC circuit for ADC input

High voltage measurement circuits require voltage division, current limiting, and over-voltage protection as shown the following figure. The voltage divider formed by R1 – R4 must yield a voltage less than or equal to VREFH. The current must be limited to less than the injection current limit. Since the ADC pins do not have diodes to VDD, external clamp diodes must be included to protect against transient over-voltages.

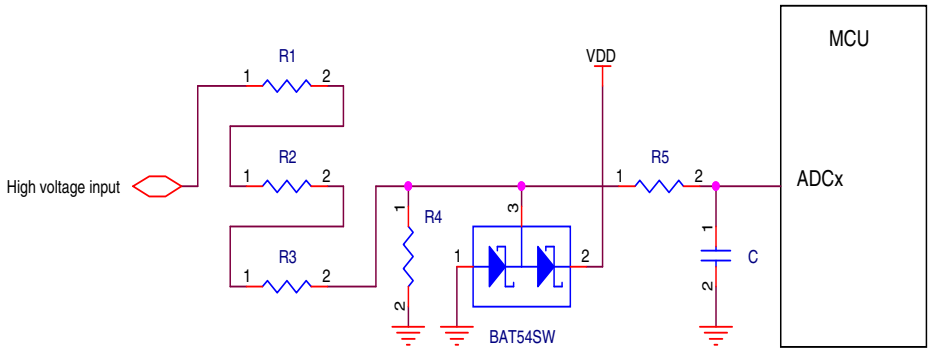


Figure 42. High voltage measurement with an ADC input

5.1.4 Digital design

Ensure that all I/O pins cannot get pulled above VDDIOx (Max I/O is VDDIOx+0.3V).

CAUTION

Do not provide power to I/O pins prior to VDDIOx, especially the RESET_b pin.

- RESET_b pin

  The RESET_b pin is an open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 μF. The RESET_b pin also has a selectable digital filter to reject spurious noise.

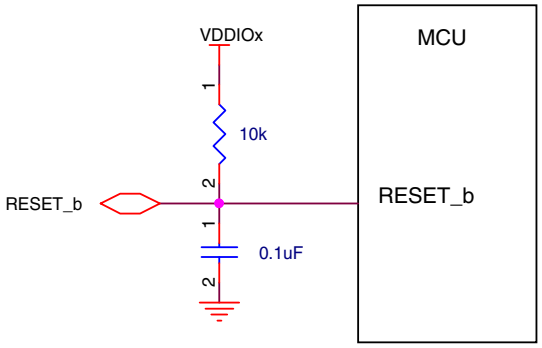


Figure 43. Reset circuit

When an external supervisor chip is connected to the RESET_b pin, a series resistor must be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in the following figure. The series resistor value (RS below) must be in the range of 100 Ω to 1 kΩ depending on the external reset chip drive strength. Select the open-drain output from the supervisor chip.

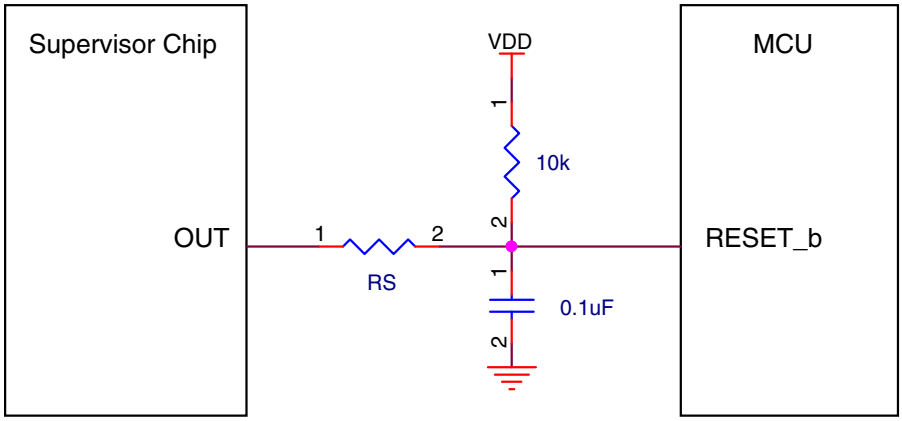


Figure 44. Reset signal connection to external reset chip

- NMI pin

  Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

  If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

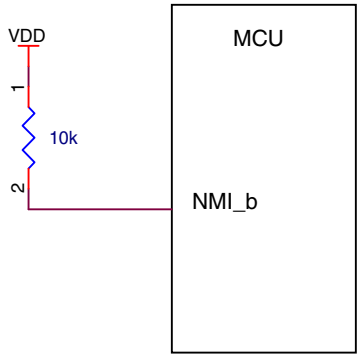


Figure 45. NMI pin biasing

- Debug interface

This MCU uses the standard Arm SWD and JTAG interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

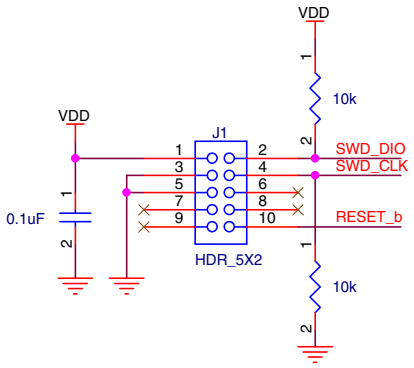


Figure 46. SWD debug interface

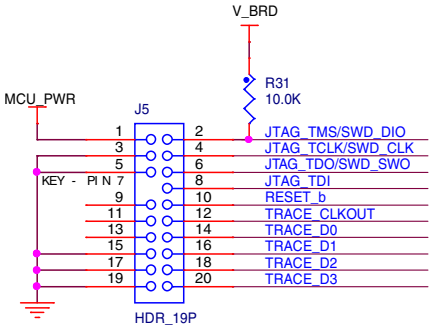


Figure 47. JTAG debug interface

- Low leakage stop mode wakeup

  Select low leakage wakeup pins (LLWU_Px) to wake the MCU from one of the low leakage stop modes (LLS/VLLSx). See K32 subfamily pinout for pin selection.

- Unused pin

  Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

  If the USB module is not used, leave the USB data pins (USB0_DP, USB0_DM) floating. Connect VREGIN and VOUT to ground through a 10 kΩ resistor if the USB module is not used.

5.1.5 Crystal oscillator

This device contains one crystal oscillator, a 32 kHz oscillator for the RTC. The output of this oscillator is available for use by other modules within the device.

The oscillator has its own integrated feedback resistor and internal load capacitors as shown in the following figure. The only external components required are the crystals. The load capacitor values for the RTC oscillator are adjusted by the SCxP bits in the CR register in the RTC module.

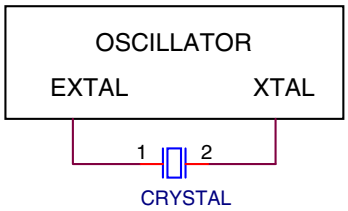


Figure 48. Crystal connection

5.2 Software considerations

All Kinetis MCUs are supported by comprehensive NXP and third-party hardware and software enablement solutions, which can reduce development costs and time to market. Featured software and tools are listed below. Visit http://www.nxp.com/kinetis/sw for more information and supporting collateral.

Evaluation and Prototyping Hardware

- Freedom Development Platform: http://www.nxp.com/freedom

IDEs for Kinetis MCUs

- MCUXpresso IDE: kex.nxp.com
- Partner IDEs: http://www.nxp.com/kide

Development Tools

- PEG Graphics Software: http://www.nxp.com/peg
- MCUXpresso Config Tools: kex.nxp.com)

Run-time Software

- Kinetis SDK: kex.nxp.com or http://www.nxp.com/ksdk

- Kinetis Bootloader: http://www.nxp.com/kboot
- Arm embed Development Platform: http://www.nxp.com/mbed

For all other partner-developed software and tools, visit http://www.nxp.com/partners.

6 Part identification

Part numbers for the device have fields that identify the specific part. Use the values of these fields to determine the specific part.

6.1 Part number format

Part numbers for this device have the following format:

B PS C FS T SPF T PG FR S PT

Table 115. Part number fields descriptions

Field	Description	Values
B	Brand	• K32
PS	Product series	• L3
C	Core	• A = M0+ and M4F
FS	Flash size	• 6 = 1.25 MB
SPF	Special feature	• 0 = Superset
T	Temperature range (°C)	• V = –40 to 105
PG	Package	• PJ = 176 VFBGA (9 mm x 9 mm)
FR	Frequency	• 1 = 50-99 MHz
S	Silicon revision	• A = Initial mask set • B = First major spin
PT	Packaging type	• R = Full reel • T = Trays • Z = Small reel

7 Revision History

The following table provides a revision history for this document.

Table 116. Revision History

Rev. No.	Date	Substantial Changes
Rev.0	06/2019	Initial release.
Rev.1	09/2019	Added Table 68.

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